Low-power dihexylquaterthiophene-based thin film transistors for analog applications

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We have optimized dihexylquaterthiophene-based thin film transistors for low-power consumption and have studied their characteristics for potential introduction in analog circuits. Bottom-gate devices with Pd source and drain electrodes have been fabricated by employing different gate dielectrics. Transistors with very thin (<10 nm) silicon oxynitride dielectrics display subthreshold swing values below 100 mV/decade, cutoff frequencies approaching the kilohertz range and intrinsic gain around 45 dB, suggesting that they are promising candidates for low-power analog integration. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2904963]

Organic thin film transistors (TFTs) have been widely investigated in the last decade, due to their promising future in pervasive applications such as radiofrequency identification tags and smart cards.[1] Out of the broad range of possible architectures and materials, bottom-gate devices on doped Si substrates, thermally oxidized and completed with source and drain electrodes, represent a very frequent choice in organic TFTs studies due to their fabrication simplicity. Unfortunately, transistors employing thick SiO_2 as gate dielectric usually require high biases to render them operational,[2,3] are susceptible of voltage-enhanced mobilities[4] and exhibit undesirable memory effects.[5,6] Generally, these shortfalls, while hampering the rapid development of hybrid organic-inorganic circuits, have fostered the introduction of highly engineered gate dielectrics.[7] Besides efficient gate insulators, key to TFTs development is the availability of high-quality, solution-processable organic semiconductors. In this context, experimental evidence has been accumulated for the existence of fast charge transport in liquid crystalline materials including thiophene derivatives by time-of-flight experiments.[8,9] A common structural feature of many studied oligothiophenes is their construction of a relatively rigid core and two flexible endgroups. The rod-shaped cores have the tendency to stack one on another, forming stable in-plane structures, hence favoring an efficient charge transport. A prototype alkyl-substituted oligothiophene used in TFTs is the dihexylquaterthiophene (DH4T).[10]

Here, we focus on the performance of DH4T transistors upon downscaling and nanoengineering of the gate insulator. We highlight the advantages of TFTs fabricated with very thin (<10 nm) silicon oxynitride SiON dielectric coated with decyltrichlorosilane (DTS) self-assembled monolayers and discuss their possible integration in low-power analog applications. While previous work[11,12] mainly reported on the saturated mobility (μ_{sat}), on-to-off current ratio ($I_{on/off}$) and threshold voltage (V_{th}), we extend the analysis to parameters essential to analog circuits such as transconductance (g_m), gain and intrinsic cutoff frequency (f_c).[13,14]

The inset to Fig. 1 schematically depicts our devices. We use 100 nm thick SiO_2 for comparison purposes with the published data. The thin gate dielectrics of interest here are 9 nm SiO_2 and 8 nm SiON and their measured capacitance values are C_i=350 and 458 nF/cm^2, respectively. The later benefits from reduced electron and hole traps with respect to SiO_2.[15] Our TFTs have Pd source and drain electrodes,[6,16] a channel width W=1000 μm and a channel length L =10 μm. To render their surfaces more hydrophobic, gate insulators have been treated with a DTS self-assembled monolayer in liquid phase, 1 h at room temperature prior to the DH4T deposition from 0.4 wt. % toluene solutions. The devices were structurally characterized by x-ray reflectometry (XRR) and electron diffraction (ED). The drain current I_d versus drain bias V_d (output) characteristics and I_d versus gate bias V_g (transfer) curves have been collected in ambient conditions.

Figure 1 displays a XRR reflectograms of drop-cast (red curve) and spin-coated (black curve) DH4T thin films deposited from 0.0075 and 0.4 wt. % toluene solutions, respectively, on 100 nm thick SiO_2 samples.[17] The Bragg peaks on both curves correspond to a vertical repeat distance of 28.5 Å. The ED data on both films (not shown here) gave an in-plane rectangular cell 6×8 Å^2 for the crystalline layers,

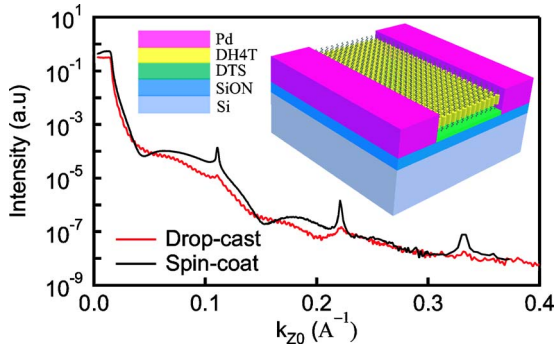

FIG. 1. (Color online) XRR data for drop-cast (red curve) and spin-coated (black curve) 80 nm thick films on SiO_2. k_{z0} is the vertical component of the wavevector in air of the incoming photons. Inset: schematics of the DH4T-based transistor architecture.

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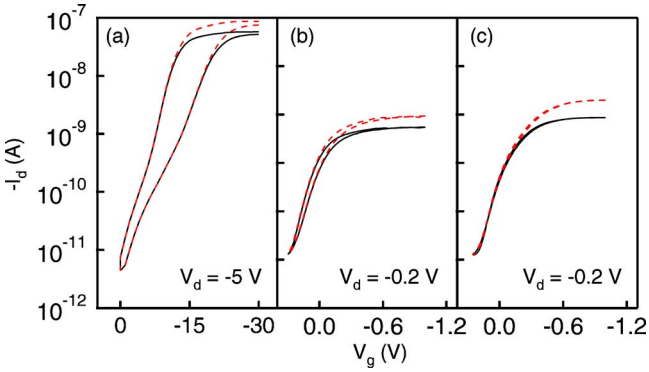

FIG. 2. (Color online) Transfer plots in the linear regime, showing the gradual reduction of the hysteresis when changing the dielectric from 100 nm SiO_2 (a), to 9 nm SiO_2 (b), and 8 nm SiON (c). The dashed red curves represent the drain current after R_{sd} correction.

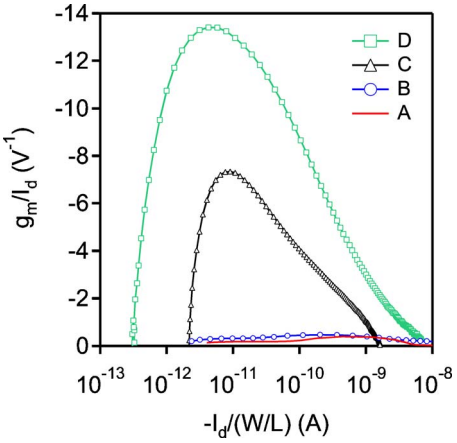

FIG. 3. (Color online) g_m/I_d vs $I_d/(W/L)$ for the transistors presented in Table I. The enhanced g_m/I_d values displayed by devices C and D (V_d=−1 V) compared to devices A and B (V_d=−30 V) corroborate with the smaller measured S values for thin SiON TFTs.

consistent with those previously reported for evaporated and spin-coated films.[11,18,19] Based on the fact that the length of the DH4T molecule is 30 Å in the most probable configuration (hexyl chains directed toward sulfur atoms), both films consist in crystalline layers of molecules oriented almost perpendicular to the substrate.

Figure 2 shows the transfer curves measured in the linear regime for three devices with different gate insulators. Devices with 100 nm SiO_2 dielectric [Fig. 2(a)] display a large hysteresis. This is generally caused by the charge trapped in the gate insulator at the insulator/organic interface or in the organic semiconductor itself.[1] Our devices likely host more trapped charges inside the SiO_2 layer than at the SiO_2/DH4T interface since transistors fabricated with 9 nm SiO_2 [Fig. 2(b)] still present hysteresis, although to a lesser extent, and coating these dielectrics with DTS results in no beneficial effect. Only for thin SiON gate insulators [Fig. 2(c)] do we observe the disappearance of hysteresis.

The performances of devices with different gate dielectrics are summarized in Table I. The V_{th} has been extracted from $I_d/g_m^{1/2}$ versus V_g plots, where $g_m=\partial I_d/\partial V_g$ is the transconductance.[20] With the aim of providing true material performance, we have focused here upon the linear mobility (μ_{lin}) and carefully considered the series resistance (R_{sd}). First, μ_{lin} was determined from the relation $I_d=(W/L)C_i\mu_{lin}(V_g-V_{th})V_d$. The R_{sd} was estimated following Ref. 21 and the drain current recalculated as $I_d^{\dagger}=I_d/(1-I_dR_{sd}/V_d)$ (dashed red curves in Fig. 2) to provide $\mu_{lin}^{\dagger}$. We have further substantiated our analysis by estimating a R_{sd}-free linear mobility $\mu_{lin}^{\ddagger}$.[22,23] As shown in Table I, the $\mu_{lin}^{\dagger}$ and $\mu_{lin}^{\ddagger}$ are in good agreement, supporting the reliability of the extracted R_{sd} values.[24] Functionalization of the inorganic gate dielectric with DTS leads to an increase of μ_{lin} above 2×10^{-2} cm^2/V s, after R_{sd} correction, in devices similar to sample D.[16] Strikingly, the subthreshold swing S decreases below 100 mV/decade for SiON/DTS dielectrics. This behavior provides another evidence that SiON/DTS devices have attracting technological attributes. The transconductance-to-drain ratio g_m/I_d versus normalized drain current $I_d/(W/L)$ is a convenient representation for comparing different devices[25] thanks to its independence on V_{th}. Figure 3 exemplifies the significant g_m/I_d improvement in the whole current range for SiON transistors (devices C and D) compared to SiO_2 TFTs and further upon DTS treatment (device D).

In the remaining, we focus on the analog parameters of our TFTs. There are scarce references to the analog performance of organic transistors[26,27] despite its crucial role when targeting circuit applications. We have calculated g_m/I_d and the Early voltage $V_{Ea}=I_d/g_d$, where $g_d=\partial I_d/\partial V_d$ is the output conductance. Two other prominent technological figures of merit[14] are the gain (g_m/g_d) and the cutoff frequency $f_c=g_m^{max}/(2\pi C_iWL)$. This f_c represents the level above which the device fails to efficiently respond, i.e., the gain deviates less than 3 dB from the nominal value. Here, g_m^{max} is the maximum transconductance obtained from plots of g_m versus V_g. For comparison purposes, the maximum normalized transconductance is defined as $g^*=g_m^{max}t/(V_g-V_{th})$, where t=8 nm is the dielectric thickness. Table II compares analog figures of merit for the devices C and D at g_m^{max} conditions.[23] Analog performance of SiON devices is clearly influenced by the presence of DTS. This can first be seen in higher g_m/I_d and hence higher gain. Values around 45 dB have been obtained in the case of transistors with SiON/DTS gate dielectric. Secondly, the DTS treatment clearly allows higher achievable transconductance values, which in turn enhance

TABLE I. Performance of TFTs fabricated with the indicated dielectrics (see text). A clear advantage of transistors with thin gate insulators is the diminished power dissipation ($V_{th}\rightarrow0$). In particular, for SiON devices the static power consumption ($I_dV_d|_{V_g=0}$) is below 1 nW. For both gate insulators, DTS coating renders in one order of magnitude improvement of $I_{on/off}$ (calculated in the saturation regime). The μ_{sat} values, as expected, are up to 30% larger than μ_{lin}.

TFT	V_{th} (V)	$I_{on/off}$	S (mV/decade)	R_{sd} (M Ω)	μ_{sat} (cm^2/V s)	μ_{lin} (cm^2/V s)	$\mu_{lin}^{\dagger}$ (cm^2/V s)	$\mu_{lin}^{\ddagger}$ (cm^2/V s)
A (100 nm SiO_2)	−10	1000	3000	30	1.7×10^{-4}	1.7×10^{-4}	2.6×10^{-4}	⋯
B (100 nm SiO_2/DTS)	−10	4×10^4	2000	2	6.5×10^{-3}	5.7×10^{-3}	1.4×10^{-2}	⋯
C (8 nm SiON)	−0.1	700	145	13	1.3×10^{-3}	1.0×10^{-3}	2.6×10^{-3}	2.7×10^{-3}
D (8 nm SiON/DTS)	0.1	2×10^4	77	6	3.8×10^{-3}	2.6×10^{-3}	1.4×10^{-2}	2.1×10^{-2}

TABLE II. Analog performance parameters for devices C and D at $V_d=-1$ V and g_m^{max} conditions.

TFT	I_d (A)	V_g (V)	g_m/I_d (V^{-1})	V_{Ea} (V)	gain (dB)	g_m^{max} (Ω^{-1})	$g^*/(W/L)$ (Ω^{-1} nm/V)	f_c (Hz)
C (8 nm SiON)	-17×10^{-9}	−0.50	−3.4	−12	32	0.5×10^{-7}	1×10^{-8}	180
D (8 nm SiON/DTS)	-41×10^{-9}	−0.15	−5.0	−37	45	1.7×10^{-7}	5×10^{-8}	600

f_c. For these transistors, we have found f_c values approaching the kilohertz range, which can be further increased by device scaling and/or diminishing R_{sd}. Finally, our SiON devices have $g^*/(W/L)$ values only few orders of magnitude lower than state-of-the-art polycrystalline silicon TFTs.[28] This suggests that a 100-fold improvement in mobility, easily conceivable in aligned liquid-crystal monodomains,[9,29] and shorter channel lengths[30] would provide devices highly appropriate for applications that especially require low-power consumption, while operating over a broad f range (from very low[31] to radio frequencies[29]).

In summary, by combining thin SiON insulators with DTS self-assembled monolayers, DH4T-based TFTs have been optimized for low-power consumption and analog applications, as exemplified by S values below 100 mV/decade and gain around 45 dB.

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