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# A Novel Design and Optimization Approach for Low Noise Amplifiers (LNA) Based on MOST Scattering Parameters and the $gm/I_D$ Ratio

Juan L. Castagnola <sup>1,\*</sup>, Fortunato C. Dualibe <sup>2</sup>, Agustín M. Laprovitta <sup>1</sup> and Hugo García-Vázquez <sup>3</sup> 

<sup>1</sup> Facultad de Ingeniería, Universidad Católica de Córdoba, Córdoba 5017, Argentina; alaprovitta@ucc.edu.ar

<sup>2</sup> Service d'Électronique et Microélectronique, Université de Mons (UMONS), 7000 Mons, Belgique; fortunato.dualibe@umons.ac.be

<sup>3</sup> Departamento de Electrónica, Instituto de Astrofísica de Canarias (IAC), 38200 La Laguna, Spain; hugo.garciavazquez@iac.es

\* Correspondence: juancastagnola@ucc.edu.ar; Tel.: +54-351-493-8087

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**Abstract:** This work presents a new design methodology for radio frequency (RF) integrated circuits based on a unified analysis of the scattering parameters of the circuit and the  $gm/I_D$  ratio of the involved transistors. Since the scattering parameters of the circuits are parameterized by means of the physical characteristics of transistors, designers can optimize transistor size and biasing to comply with the circuit specifications given in terms of S-parameters. A complete design of a cascode low noise amplifier (LNA) in MOS 65 nm technology is taken as a case study in order to validate the approach. In addition, this methodology permits the identification of the best trade-off between the minimum noise figure and the maximum gain for the LNA in a very simple way.

**Keywords:** LNA design;  $gm/I_D$ ; ACM; S-parameters; methodology; optimization

## 1. Introduction

The low noise amplifier (LNA) is considered a crucial component in wireless communication systems. Since it is the first stage of the receiver, the LNA design characteristics (such as high-gain, low-noise figure, linearity) condition the reception performance of the whole system [1]. However, it is a fact that in radio frequency (RF) design, it is very difficult to meet all the specifications simultaneously because of the large number of constraints to be satisfied. Broadly, there are two approaches to designing an LNA, depending on the critical specification to be addressed: looking for the maximum gain or the minimum noise figure. The traditional high frequency MOS design flow is tedious, time-consuming, and usually relies on the designer's experience. This supposes conducting an iterative process, generally assisted by a CAD simulation tool, until the design specifications are satisfied.

In order to characterize these kinds of circuits, the scattering parameters (or S-parameters) are the most likely symbolic approach, where signal power considerations are more easily quantified and measured than currents and voltages. These parameters reflect the power gain and the input and output matching of the circuit. However, there is no model that relates S-parameters to the physical characteristics of the transistors, which represent the main variables to consider in order to address the aforementioned LNA design constraints [2].

On one hand, the advanced compact MOSFET (ACM) model [3] is a powerful tool for hand calculations with MOS transistors. Unlike most of the available models, it presents simple and precise equations together with a small but meaningful number of physics parameters. On the other hand, the relationship between the transistor's transconductance ( $gm$ ) and the drain current ( $I_D$ ), also known

as the  $gm/I_D$  ratio, is widely used as a design methodology for determining the transistor's size [4]. This method is based on the dependence of both the transconductance and the current with the variation of the transistor size ( $W/L$ ). Through this method, it is possible to explore the transistor's behavior in all its inversion regions [5,6]. Consequently, an LNA design methodology based on a unified analysis of the S-parameters and the  $gm/I_D$  ratio, by means of the ACM model, will allow designers to set the transistor sizes and bias conditions that best fit the design expectations.

Several approaches can be found in the literature reporting integrated LNA design methodologies, with different strategies regarding the parameters analyzed in the design process [7–16]. An even larger quantity of different configurations has been proposed for specific applications [17–26]. For example, in [7,17–22] different LNA topologies using diverse design flows are presented, but all use the S-parameters exclusively for verification purposes.

In [27], an interesting two-step design methodology is presented that generates a set of inductors with the best trade-offs using iterative electromagnetic simulations. Inductors are selected from the Pareto frontier, and its S-parameter matrix is included in the circuit to be simulated. This approach eliminates the classical redesign iterations; however, it does not address the problem of transistor sizing. On the other hand, [28] reports a portable design methodology based on a low-power figure of merit ( $FOM$ ) and inversion coefficient ( $IC$ ). The  $IC$  is a normalization of the MOS drain current that allows a description of the transistor behavior independently of its technological parameters. Although this method solves the problem of the physical characterization of the amplifier core using the  $gm$  parameter and the bias currents, the S-parameters are used independently to verify if the targeted specification was reached at each iteration loop.

The characterization of an LNA common source (CS) stage in terms of the S-parameters, the  $gm/I_D$  ratio and the transistor's size, was introduced for the first time in [29]. In [30], this approach is extended to the whole design of an LNA. Based on these authors' previous works, this paper presents a comprehensive description of such a methodology for RF circuit design. In this strategy, the S-parameters of the circuit are parameterized by means of the MOS  $gm/I_D$  ratios, allowing designers to choose the latter in order to optimize transistor size and bias to comply with the circuit specifications. The design space exploration of a complete cascode LNA in CMOS 65 nm technology is reported, considering the amplifier gain ( $G$ ), noise figure ( $NF$ ), and stability Stern factor ( $K$ ) as its most relevant design specifications. In addition, this approach allows the identification of the best trade-off between the minimum noise figure and maximum gain for the LNA in a very simple way.

This work is based on the relationship between hybrid and Y-parameters in order to give a theoretical background, while demonstrating the link between S-parameters and the  $gm/I_D$  ratio of transistors. It should be noted, however, that the central idea is that the designer directly uses the S-parameters expressed in terms of the  $gm/I_D$  ratio extracted from simulations or, more realistically, from measurements on real transistors previously implemented in a test chip.

The remainder of this work is organized as follows: in Section 2, the relationships between the S-parameters and the physical transistor (ACM model) are established. A complete LNA design process is described as a case study in Section 3, where its available power gain and noise figure are characterized as a function of the transistors'  $gm/I_D$ . Finally, Section 4 concludes the paper.

## 2. Design Approach: Linking the Circuit S-Parameters with the $gm/I_D$ Transistor Ratio

The  $gm/I_D$  ratio is a resourceful tool for performing transistor sizing and biasing. As mentioned earlier, this method exploits the fact that transconductance and drain currents vary with the gate width. From the design perspective, the  $gm/I_D$  ratio is the parameter that tells the designer how much current is needed to obtain a particular  $gm$ , prescribed by the gain-bandwidth constraint.

Figure 1 shows the well-known  $I_D$  versus  $V_{gs}$  characteristics of a NMOS transistor. From this curve, one can obtain the  $gm/I_D$  ratio as follows:

$$\left(\frac{gm}{I_D}\right) = \frac{1}{I_D} \cdot \frac{dI_D}{dV_G} = \frac{d}{dV_G} \log(I_D) \quad (1)$$

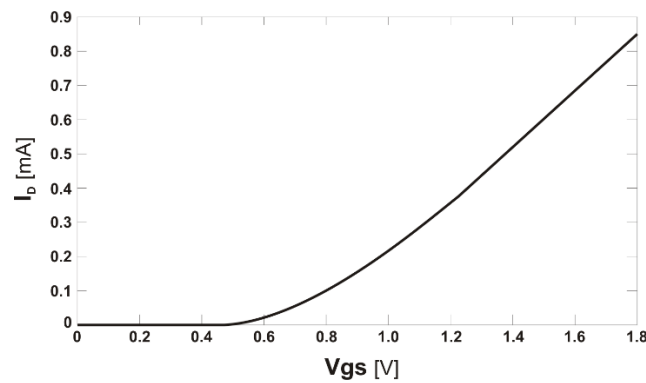


Figure 1.  $I_D$  versus  $V_{gs}$ .

The above equation is plotted in Figure 2. From Equation (1), it can be noted that the  $gm/I_D$  ratio does not depend on the gate width but on the inversion region where the transistors are biased. As seen in Figure 2, the  $gm/I_D$  is at its maximum when the  $V_{gs}$  is at its minimum. This is because the  $gm/I_D$  is inversely proportional to the gate-voltage-overdrive  $V_{ov} = V_{gs} - V_{th}$ . Based on the value of  $V_{gs}$ , the MOS transistor can operate in three different regions: weak, moderate, and strong inversion. In the first region, the value of the  $gm/I_D$  is at its maximum, while its minimum is in strong inversion. Conversely, the current is at its maximum in strong inversion and at its minimum in weak inversion, as shown in Figure 1.

A more useful plot is shown in Figure 3, in which the  $gm/I_D$  ratio is plotted as a function of the normalized current  $i_D$ , which is given by:

$$i_D = \frac{I_D}{\left(\frac{W}{L}\right)} \tag{2}$$

In this way, its position along the horizontal axis of the  $gm/I_D$  curve becomes independent of the threshold voltage  $V_{th}$ . For a given  $I_D$  and a desired operation region ( $gm/I_D$ ), the transistor size is easily obtained as the following:

$$W/L = \frac{I_D}{i_D} \tag{3}$$

At the same time, through the curve in Figure 2, one can obtain the needed  $V_{gs}$  biasing voltage. In short, the  $gm/I_D$ ,  $i_D$ , and  $V_{gs}$  form a trinity that defines the transistor working conditions. Knowing the value of one of these values and using the curves in Figures 2 and 3, the values of the other two can be inferred.

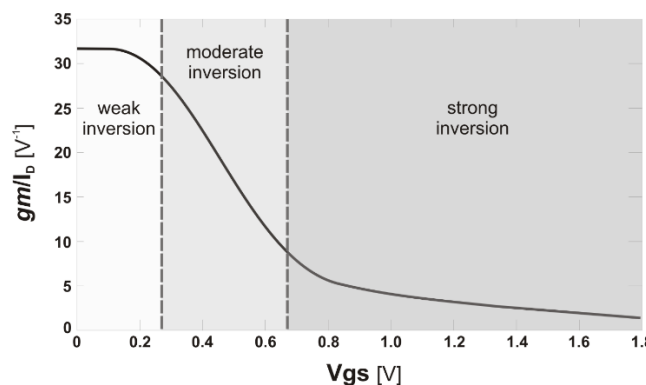


Figure 2.  $gm/I_D$  versus  $V_{gs}$ .

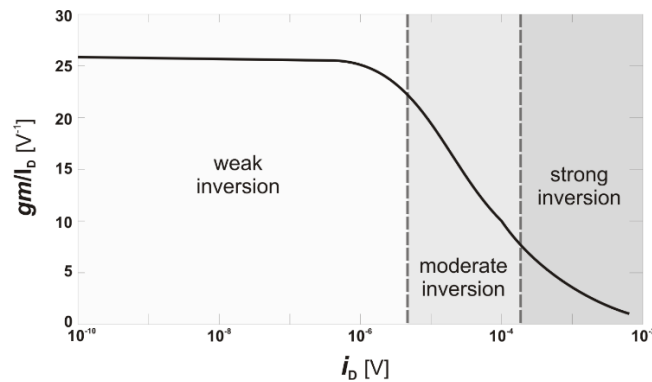


Figure 3.  $gm/I_D$  versus  $i_D$ .

The key idea is to use the  $gm/I_D$  ratio as a free parameter that enables sweeping the transistor through all modes of operation in order to explore the design space. Broadly, there are two working methodologies: experimental or analytical. The first derives the  $gm/I_D$  ratio from experimental  $I_D = f(V_{gs})$  characteristics. The currents are acquired from measurements carried out on real transistors whose  $W$  and  $L$  are known a priori. Another option is to obtain the  $I_D$  from simulations with advanced models, such as BSIM or PSP4, as these allow the reconstruction of drain currents that are very close to real ones. The last option is also known as the semi-empirical  $gm/I_D$  sizing method.

This LNA design approach is based on the analysis of the variation in the circuit S-parameters as a function of the physical transistor ( $gm/I_D$ ). Thus, it is necessary to link the transistor geometry and biasing conditions (expressed in terms of the  $gm/I_D$  ratio) with the design specifications given in terms of the S-parameters. In this direction, the expressions given by the ACM model for the full characterization of the MOS transistors [3,8] can be used. Figure 4 shows the RF small signal equivalent circuit for an MOS transistor with intrinsic and extrinsic components depicted separately.

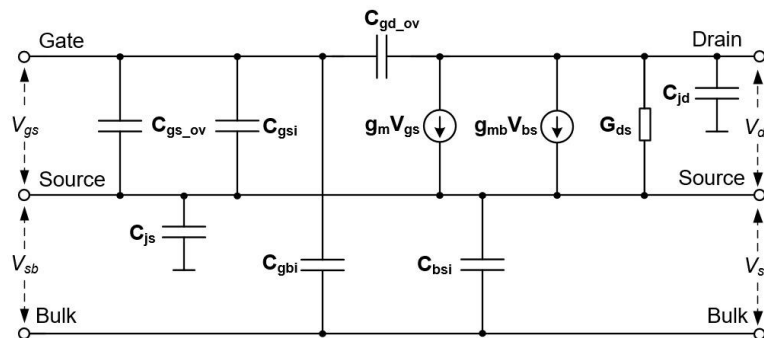


Figure 4. MOS radio frequency (RF) small signal equivalent circuit.

From the ACM model, it is possible to obtain the expressions of the intrinsic capacitances in terms of the  $gm/I_D$  transistor ratio. The latter are synthesized in Table 1, while Table 2 reports the expressions for the extrinsic capacitances. In these expressions,  $W$  is the channel width,  $L$  is the channel length,  $\Phi_t$  is the thermal voltage,  $C_{OX}$  is the gate capacitance density,  $C_{OV}$  is the overlap capacitance density, and  $C_j'$  is the junction capacitance density. Table 3 shows the definition of the gate and bulk transconductance ( $gm$  and  $gmb$ , respectively) and the drain conductance ( $gds$ ), which can also be expressed as a function of the MOS  $gm/I_D$ . In this case,  $n$  is the subthreshold slope factor, and  $V_A$  represents the early voltage.

**Table 1.** MOS intrinsic capacitance expressions.

Parameter	Expression
Auxiliary expression	$A = \frac{(g_m/I_D)}{(g_m/I_D)_{MAX}}$
Intrinsic gate-source capacitance	$C_{gsi} = \frac{2}{3}C_{ox} \cdot W \cdot L \left(1 - \frac{1}{2}A - \frac{1}{2}A^2\right)$
Intrinsic gate-bulk capacitance	$C_{gbi} = \left(1 - (g_m/I_D)_{MAX} \cdot \Phi_t\right) \frac{C_{ox} \cdot W \cdot L}{3} (1 + A + A^2)$
Intrinsic bulk-source capacitance	$C_{bsi} = \left(\frac{1}{(g_m/I_D)_{MAX} \cdot \Phi_t} - 1\right) \frac{2}{3}C_{ox} \cdot W \cdot L \left(1 - \frac{1}{2}A - \frac{1}{2}A^2\right)$

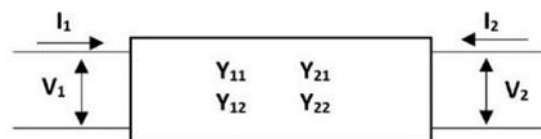
**Table 2.** MOS extrinsic capacitance expressions.

Parameter	Expression
Extrinsic gate-drain overlap capacitance	$C_{gd_{ov}} = W \cdot C_{ov}$
Intrinsic gate-source capacitance	$C_{gs_{ov}} = W \cdot C_{ov}$
Intrinsic gate-bulk capacitance	$C_{jd} = W \cdot L_{Diff} \cdot C_j'$
Intrinsic bulk-source capacitance	$C_{js} = W \cdot L_{Diff} \cdot C_j'$

**Table 3.** MOS transconductance and conductance expressions.

Parameter	Expression
Gate small signal transconductance	$gm = \frac{\partial I_{DS}}{\partial V_{gs}} = \left(\frac{gm}{ID}\right) I_D$
Body small signal transconductance	$gmb = \frac{\partial I_{DS}}{\partial V_{bs}} = (1 + n)gm$
Output small signal conductance	$gds = \frac{\partial I_{DS}}{\partial V_{ds}} = \frac{V_A}{I_D}$

When the transistor modelled in Figure 4 is part of a more complex circuit arrangement with other external components, this arrangement can be represented as a quadrupole (shown in Figure 5), and its admittance parameters ( $Y_{ij}$ ) can be derived from the complete circuit using a two-port model. Then, each Y-matrix element will be a function of the aforementioned MOS elements (capacitances, conductance, and transconductance) and the involved external components. These admittance parameters are used as an intermediate step for obtaining the S-parameters.



**Figure 5.** Admittance two-port circuit model.

Finally, the S-parameters can be easily obtained from the admittance matrix [31], as follows:

$$S_{11} = \frac{[(Y_0 - Y_{11}) \cdot (Y_0 + Y_{22}) + Y_{12} \cdot Y_{21}]}{(Y_0 + Y_{11}) \cdot (Y_0 + Y_{22}) - Y_{12} \cdot Y_{21}} \tag{4}$$

$$S_{12} = \frac{-2 \cdot Y_{12} \cdot Y_0}{(Y_0 + Y_{11}) \cdot (Y_0 + Y_{22}) - Y_{12} \cdot Y_{21}} \tag{5}$$

$$S_{21} = \frac{-2 \cdot Y_{21} \cdot Y_0}{(Y_0 + Y_{11}) \cdot (Y_0 + Y_{22}) - Y_{12} \cdot Y_{21}} \tag{6}$$

$$S_{22} = \frac{[(Y_0 + Y_{11}) \cdot (Y_0 - Y_{22}) + Y_{12} \cdot Y_{21}]}{(Y_0 + Y_{11}) \cdot (Y_0 + Y_{22}) - Y_{12} \cdot Y_{21}} \tag{7}$$

Figure 6 summarizes the procedure for obtaining the circuit’s S-parameters as a function of the physical properties of the transistor. A validation of these relations can be found in [29], where this strategy was applied to the characterization of an LNA common source stage, and concurrent simulations with the ACM and IBM BSIM4 MOS 65 nm models were performed.

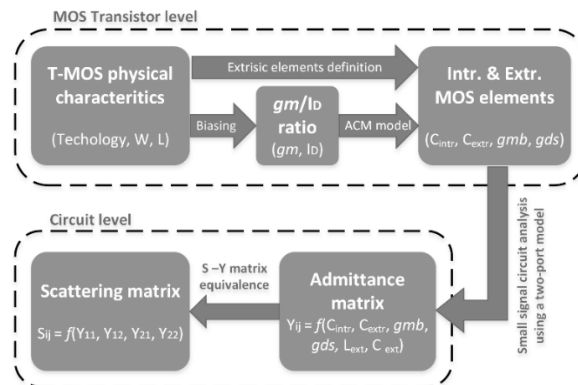


Figure 6. Procedure for obtaining S-parameters by means of the MOS physical characteristics.

### 3. LNA Design Methodology

The selected LNA configuration, shown in Figure 7, corresponds to a cascode topology. It consists of the transistors, M1 and M2, in common source and common gate configuration, respectively, which fix the gain of the LNA. C1 and L1 set a stabilization network that ensures that the amplifier is unconditionally stable. The C2–L2 pair is part of the input-matching network, setting the input impedance to 50 ohms at the working frequency. C3–L3 is the output-matching network. The rest of the circuit (M3, R1, and R2) form the bias network that sets the LNA bias conditions ( $V_{gs}$  and  $I_D$  at M1).

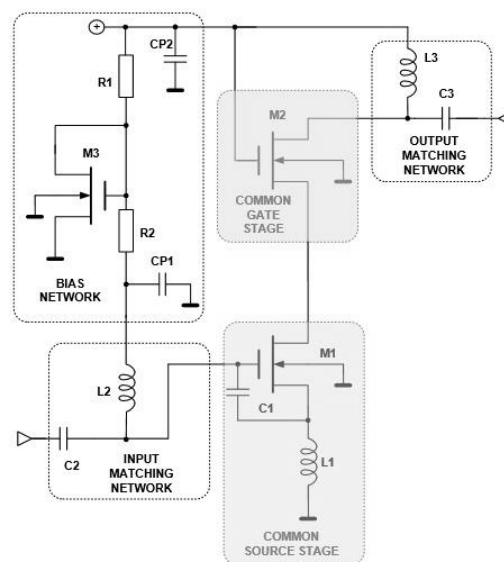


Figure 7. Cascode low noise amplifier (LNA) block diagram.

It is worth noting that the analysis of the admittance matrix must be individually performed for each LNA stage. This is because the transistor configuration is different at each stage and, consequently, the involved elements of the small signal transistor model will also be different for each of them. As mentioned above, the presence of external components must be considered. This work focuses on the amplifier core, consisting of the common source (CS) stage and the common gate (CG) stage, highlighted in Figure 7. For the sake of clarity, the general expressions of the Y-matrix elements

for the CS stage as a function of the MOS physical characteristics and bias conditions are presented (Equations (8) to (11)). The admittance matrix for the CG stage can be ascertained in the same way.

$$Y_{11\_CS} = \frac{S \cdot C_{gs} \cdot (Y_{SB} + g_{mb} + G_{ds})}{S \cdot C_{gs} + Y_{SB} + g_m + g_{mb} + G_{ds}} + S \cdot (C_{gbi} + C_{gd\_ov}) \tag{8}$$

$$Y_{12\_CS} = -\frac{S \cdot C_{gs} \cdot G_{ds}}{S \cdot C_{gs} + Y_{SB} + g_m + g_{mb} + G_{ds}} + S \cdot C_{gd\_ov} \tag{9}$$

$$Y_{21\_CS} = -\frac{S \cdot C_{gs} \cdot G_{ds} + S \cdot C_{gs} \cdot g_{mb} - Y_{SB} \cdot g_m}{S \cdot C_{gs} + Y_{SB} + g_m + g_{mb} + G_{ds}} + S \cdot C_{gd\_ov} \tag{10}$$

$$Y_{22\_CS} = \frac{G_{ds} \cdot (Y_{SB} + S \cdot C_{gs})}{S \cdot C_{gs} + Y_{SB} + g_m + g_{mb} + G_{ds}} + S \cdot (C_{gbi} + C_{gd\_ov}) \tag{11}$$

In these expressions,  $Y_{SB}$  is the MOS source-bulk admittance, and  $C_{gs}$  represents the gate-source capacitance. Both are defined as follows:

$$Y_{SB} = S \cdot (C_{jd} + C_{gd\_ov}) + \frac{1}{S \cdot L_1} \tag{12}$$

$$C_{gs} = C_1 + C_{gsi} + C_{gs\_ov} \tag{13}$$

The procedure, depicted in Figure 8, starts with the analysis of each LNA’s stage. For each, the variation of the transistor drain current ( $I_D$ ) and transconductance ( $gm$ ) with its size and bias voltage ( $V_{GS}$  for CS and  $V_{GG}$  for CG) is determined by simulation. With both functions, the MOS  $gm/I_D$  ratio is then established. Using the relationships found in the second section (Tables 1–3 and Equations (4) to (7)), the S-parameters are characterized as a function of the transistor’s  $gm/I_D$  and size.

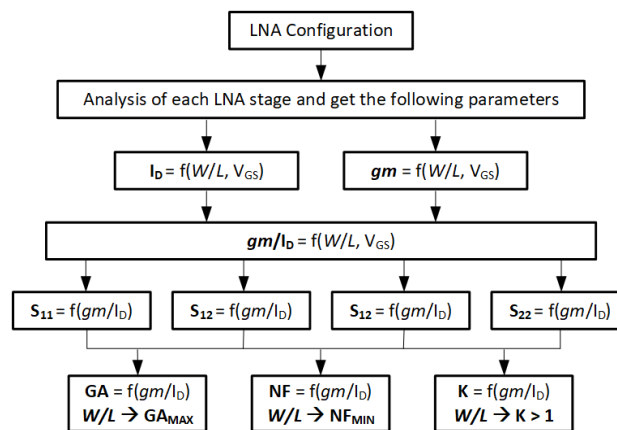


Figure 8. LNA stage characterization procedure.

The gain, noise figure, and stability factor of each stage can be easily derived from its S-parameters, allowing the design space exploration of such parameters as a function of the  $gm/I_D$  ratio and the transistor geometry. In this way, the designer sizes the MOS transistor by simply selecting the gain and noise figure points that best fit with the stage requirement and by verifying stability with the  $K$  factor.

The S-matrix of the whole amplifier can be expressed as the result of the cascade of two quadrupoles (CS and CG stages), each characterized by its individual S-matrix. With this new S-matrix, it should be verified that the amplifier complies with the gain and noise figure specifications. The next subsections provide further details about the complete design procedure. The circuit was characterized in an MOS 65 nm technology for a 2440 MHz operation frequency. Simulations were performed with Microwave Office (MWO)-AWR using the IBM BSIM4 model.

### 3.1. Common Source (CS) Stage Characterisation

Figure 9 shows the simulation setup for the common source stage. As stated earlier, the elements C1 and L1 were added to the circuit in order to ensure the stability of the amplifier. The S-parameters are obtained as a function of the  $gm/I_D$  performing parametric AC simulation by varying the  $W/L$  in the range of 1000 and 5750 in steps of 250, and the  $V_{gs}$  between 600 and 1075 mV in steps of 25 mV.

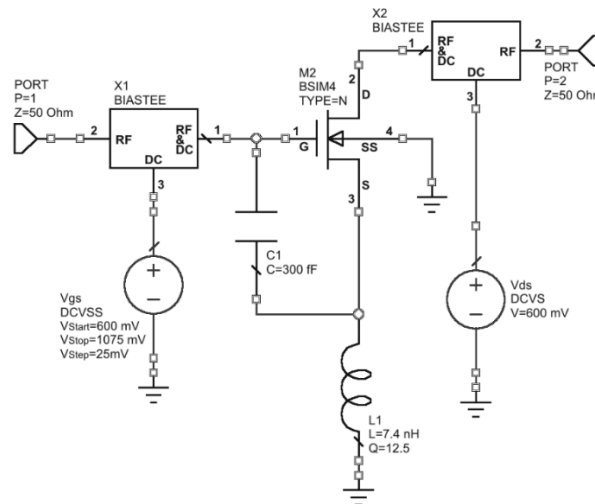


Figure 9. Common source (CS) stage schematic circuit used for characterization.

The available power gain ( $GA$ ), defined as the ratio between the available power at the output network ( $P_N$ ) and the available power from the source ( $P_S$ ), is given by the following:

$$GA = \frac{P_N}{P_S} = \frac{1 - |\Gamma_s|^2}{|1 - S_{11} \cdot \Gamma_s|^2} \cdot |S_{21}|^2 \cdot \frac{1}{1 - \left| S_{22} + \frac{S_{12} \cdot S_{21} \cdot \Gamma_s}{1 - S_{11} \cdot \Gamma_s} \right|^2} \quad (14)$$

In the above equation,  $\Gamma_s$  must be zero at the maximum gain. In this condition, the  $GA$  depends only on the S-parameters that can be expressed in terms of the transistor  $gm/I_D$ . Consequently, Equation (14) now becomes:

$$GA_{CS} = \left| S_{21\_CS}((gm/I_D)_{CS}) \right|^2 \cdot \frac{1}{1 - \left| S_{22\_CS}((gm/I_D)_{CS}) \right|^2} \quad (15)$$

Figure 10a reports the result for the  $GA_{CS}$  as a function of the  $gm/I_D$  ratio for different transistor sizes. The maximum  $GA_{CS}$  is 10.71 dB for a  $gm/I_D$  of  $13.39 \text{ V}^{-1}$  and a  $W/L$  ratio of 1000. Similarly, the noise figure for the CS stage is depicted in Figure 10b. The minimum  $NF_{CS}$  is 0.9076 dB for a  $gm/I_D$  of  $13.11 \text{ V}^{-1}$  and a  $W/L$  ratio of 2000. As can be verified from Figure 10c, the circuit with the stabilization network C1–L1 is unconditionally stable since the  $K$  factor is greater than one in all cases.

### 3.2. Common Gate (CG) Stage Characterisation

The same procedure is executed in order to obtain the S-parameters for the common gate configuration (see Figure 11). It should be noted that this configuration does not need extra components to warrant the stability of the circuit. As in the previous case, the simulation was performed varying the  $W/L$  between 1000 and 5750 in steps of 250, but the  $V_{gg}$  was in the range between 1210 and 1400 mV in steps of 10 mV.



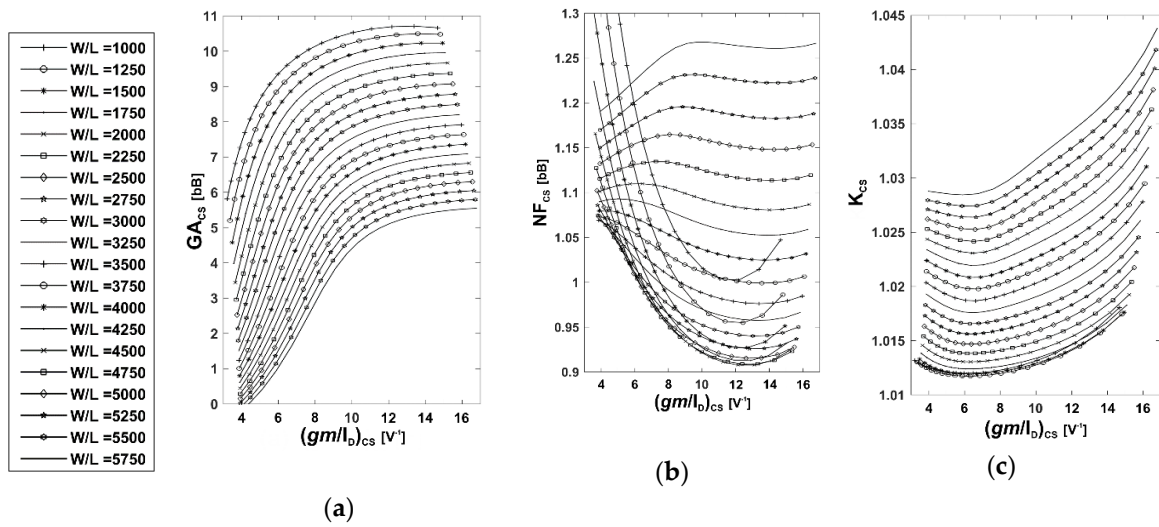


Figure 10. CS stage response as a function of the  $gm/I_D$ : (a) gain; (b) noise figure; (c) stability factor  $K$ .

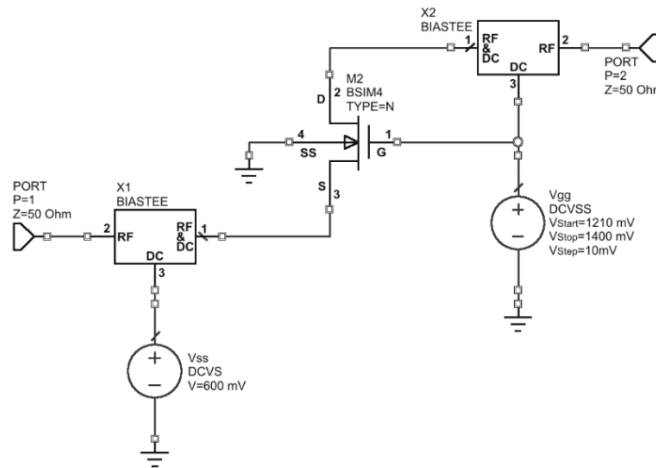


Figure 11. Common gate (CG) stage schematic circuit used for characterization.

The  $GA_{CG}$  expression in terms of the S-parameters and transistor  $gm/I_D$  is given by the following:

$$GA_{CG} = \left| S_{21\_CG}((gm/I_D)_{CG}) \right|^2 \cdot \frac{1}{1 - \left| S_{22\_CG}((gm/I_D)_{CG}) \right|^2} \tag{16}$$

The available gain is plotted in Figure 12a for different  $W/L$  ratios. The maximum  $GA_{CG}$  is 9.76 dB for a  $gm/I_D$  of  $12.41 \text{ V}^{-1}$  with a  $W/L$  ratio of 3250. Figure 12b shows the  $NF_{CG}$  for different  $W/L$  ratios. The minimum noise figure of this stage is 1.335 dB for a  $gm/I_D$  of  $13.85 \text{ V}^{-1}$  and a  $W/L$  ratio of 5750. Finally, Figure 12c confirms that the configuration is unconditionally stable, with  $K$  always greater than one.

As can be seen from the analysis of each stage, the optimal condition of the MOS transistor geometry and bias diverges depending on the design focus. At this point, the designer should set the transistors'  $W/L$  ratios and bias conditions that best fit with the LNA performance specifications and in agreement with the design focus. Both the maximum gain and the minimum noise figure will be analyzed in the next subsection for demonstration purposes.

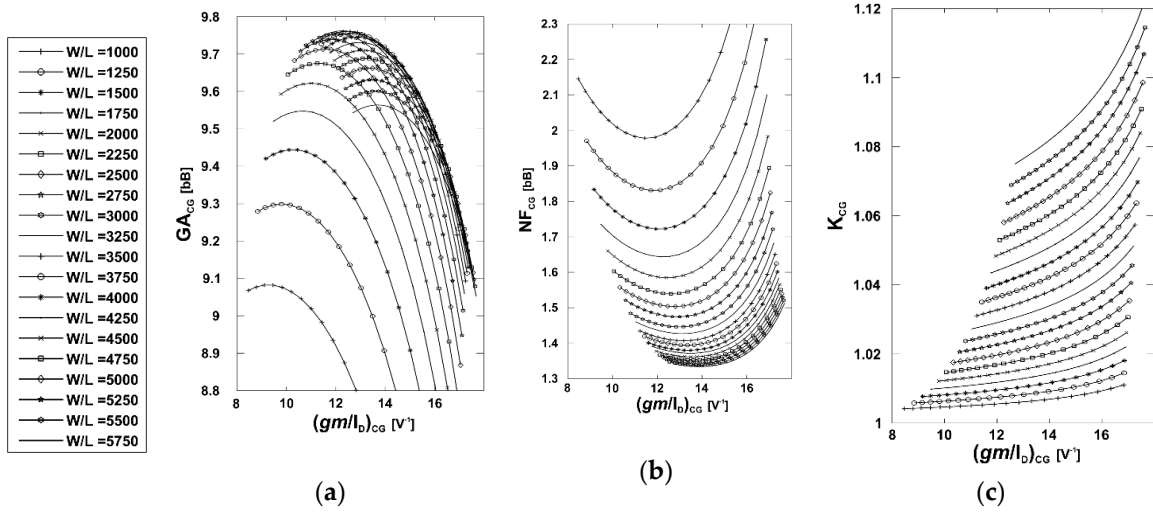


Figure 12. CG stage response as a function of the  $gm/I_D$ : (a) gain; (b) noise figure; (c) stability factor  $K$ .

### 3.3. Cascode Characterisation

Once the CS and CG stages have been individually characterized by their S-matrices, the S-parameters of the cascode topology can be expressed as the result of the cascade connection of two quadrupoles [31]. In this way, each S-matrix element of the cascode stage is given as follows:

$$S_{11\_Cascode} = S_{11\_CS} + \frac{S_{12\_CS} \cdot S_{11\_CG} \cdot S_{21\_CS}}{1 - S_{11\_CG} \cdot S_{22\_CS}} \quad (17)$$

$$S_{12\_Cascode} = \frac{S_{12\_CS} \cdot S_{12\_CG}}{1 - S_{11\_CG} \cdot S_{22\_CS}} \quad (18)$$

$$S_{21\_Cascode} = \frac{S_{21\_CS} \cdot S_{21\_CG}}{1 - S_{11\_CG} \cdot S_{22\_CS}} \quad (19)$$

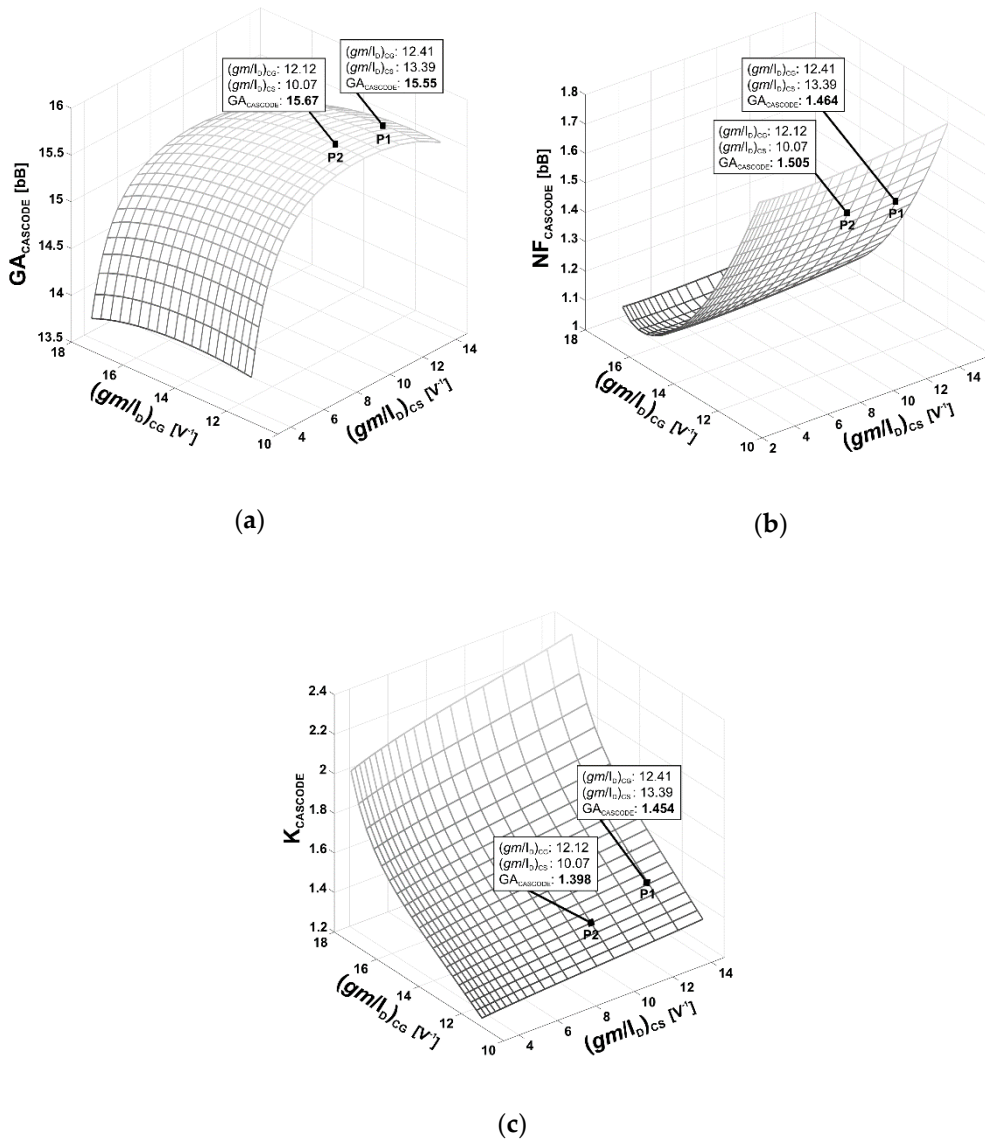
$$S_{22\_Cascode} = S_{22\_CS} + \frac{S_{12\_CG} \cdot S_{22\_CS} \cdot S_{21\_CG}}{1 - S_{11\_CG} \cdot S_{22\_CS}} \quad (20)$$

With the  $W/L$  ratios of the above stages fixed according to the design criteria, the cascode S-parameters can be analyzed as a function of the  $gm/I_D$  of both transistors. The cascode gain parameter, given by Equation (21), can be processed in the same way.

$$GA_{CASCODE} = |S_{21\_CASCODE}|^2 \cdot \frac{1}{1 - |S_{22\_CASCODE}|^2} \quad (21)$$

First, the design procedure will be explained in order to obtain the maximum LNA gain. The available power gain area in Figure 13a has been generated for a  $(W/L)_{CS}$  ratio of 1000 and a  $(W/L)_{CG}$  ratio of 3250, which correspond to the transistor sizes for the maximum gain of each stage. The  $GA_{CASCODE}$  is presented as a function of the  $gm/I_D$  of each configuration in order to determine the exact polarization points that set the maximum gain condition.

If the polarization conditions for the maximum gain in each stage (shown as P1 in Figure 13) are evaluated, the available power gain of the cascode configuration results in 15.55 dB. However, the point of the maximum power gain is 15.69 dB, and corresponds to a  $(gm/I_D)_{CS}$  of  $10.07 \text{ V}^{-1}$  and a  $(gm/I_D)_{CG}$  of  $12.12 \text{ V}^{-1}$  (labelled as P2). This small shift in the bias conditions derives from an internal impedance mismatch in the cascode connection of both stages. These new adjusted values will be those used in the next design processes, focusing on the maximum gain constraint.



**Figure 13.** Plot of the cascode stage response for the maximum gain condition, as a function of the  $(gm/I_D)_{CS}$  and  $(gm/I_D)_{CG}$ : (a) gain; (b) noise figure; (c) stability factor  $K$ .

An analysis of the noise figure behavior of the cascode configuration was performed for the above-described conditions, and the results are shown in Figure 13b. This graph is obtained by using the Friis equation [32] for the noise factor:

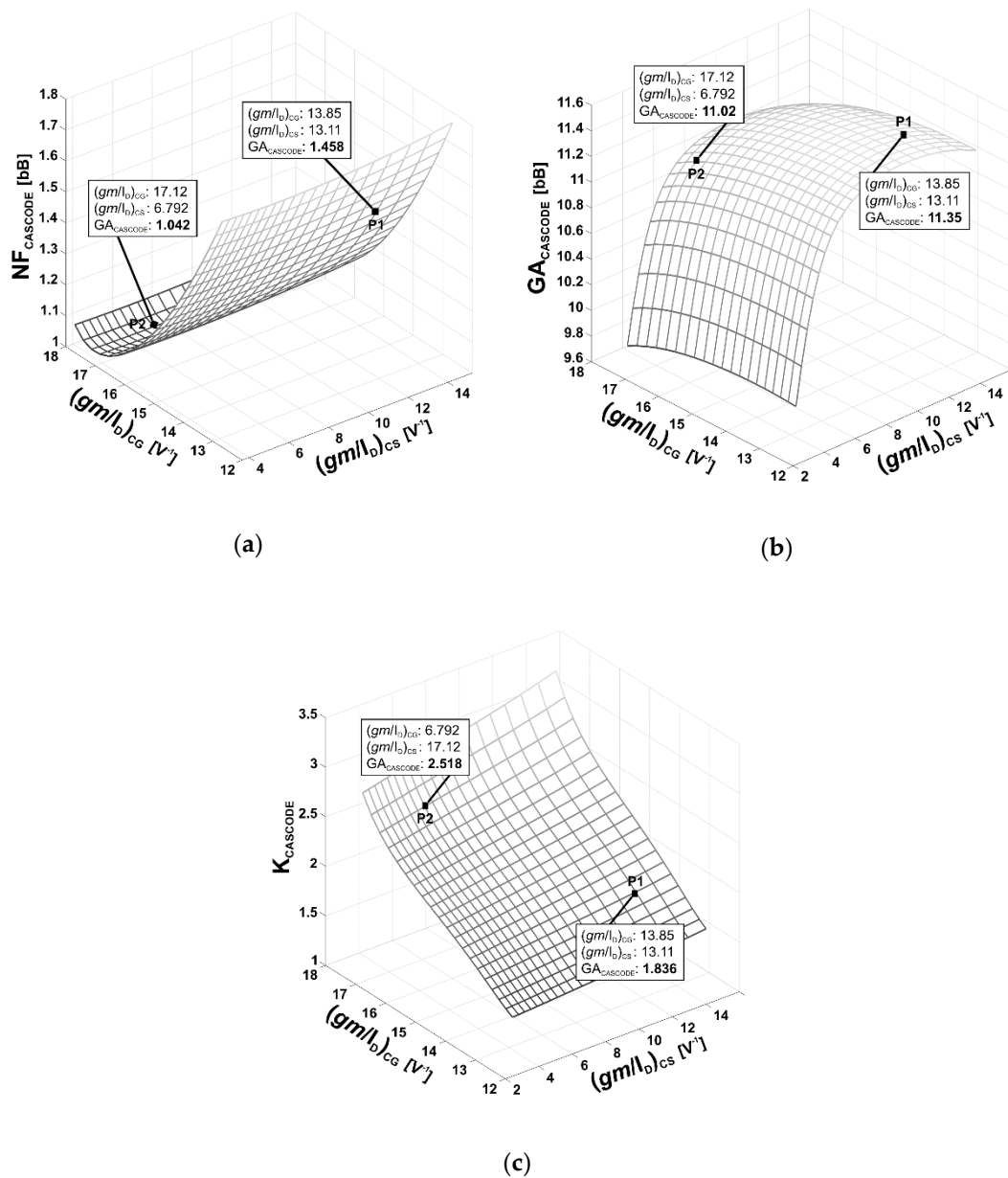
$$F_T = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \cdot G_2} + \dots + \frac{F_N - 1}{G_1 \cdot G_2 \cdot \dots \cdot G_{N-1}} \quad (22)$$

It can be noted that the total noise ( $F_T$ ) depends on the noise of each stage ( $F_i$ ) and gain of the previous stages ( $G_{i-1} \dots G_{N-1}$ ). For the cascode arrangement, Equation (22) is reduced to the following:

$$NF_{CASCADE} = 10 \cdot \log \left( F_{CS} + \frac{F_{CG} - 1}{GA_{CS}} \right) \quad (23)$$

Figure 13c reports the behavior of the stability factor  $K$  as a function of the  $gm/I_D$  of each stage. In the evaluated points (P1 and P2), the cascode configuration is still unconditionally stable for the maximum gain condition.

Conversely, if the design had been approached following the noise criteria, the correct decision would have been to minimize the noise figure at the CS and the CG stages. Using the same procedure as in the previous case, an analysis of the noise behavior of the cascode stage is performed for a  $(W/L)_{CS}$  of 2000 and a  $(W/L)_{CG}$  ratio of 5750, which correspond to the transistor sizes obtained for the minimum noise figure in the CS and CG stages' characterizations. Figure 14a summarizes the simulation results, showing the  $NF_{CASCODE}$  as a function of the  $gm/I_D$  of each transistor.



**Figure 14.** Plot of the cascode stage response for the minimum noise figure, as a function of the  $(gm/I_D)_{CS}$  and  $(gm/I_D)_{CG}$ : (a) noise figure; (b) gain; (c) stability factor  $K$ .

The minimum  $NF_{CASCODE}$  is 1.042 dB, found for a  $(gm/I_D)_{CS}$  of 6.792  $V^{-1}$  and a  $(gm/I_D)_{CG}$  of 17.120  $V^{-1}$  (P2 in Figure 14a). This polarization condition generates an available power gain of 11.02 dB (see P2 in Figure 14b). As in the case of the maximum gain, the minimum noise figure is shifted with respect to the polarization conditions set in the characterization of the individual stages (denoted as P1 in Figure 14) due to the internal impedance mismatch in the cascode connection. Figure 14c describes

how stable the circuit is, depending on the bias condition of each stage. These graphs verify that the stability factor  $K$  increases as the noise figure decreases.

### 3.4. Complete LNA Circuit

Once the physical parameters of the cascode amplifier have been established, the LNA design is completed with the input and output matching networks and the bias network sections (see Figure 7). The latter sets the gate-source voltage ( $V_{gs}$ ) of the CS transistor, which determines the bias condition of the entire cascode arrangement, while the former allows the LNA to achieve the maximum energy transfer. Only the maximum power gain analysis is taken into consideration at this stage.

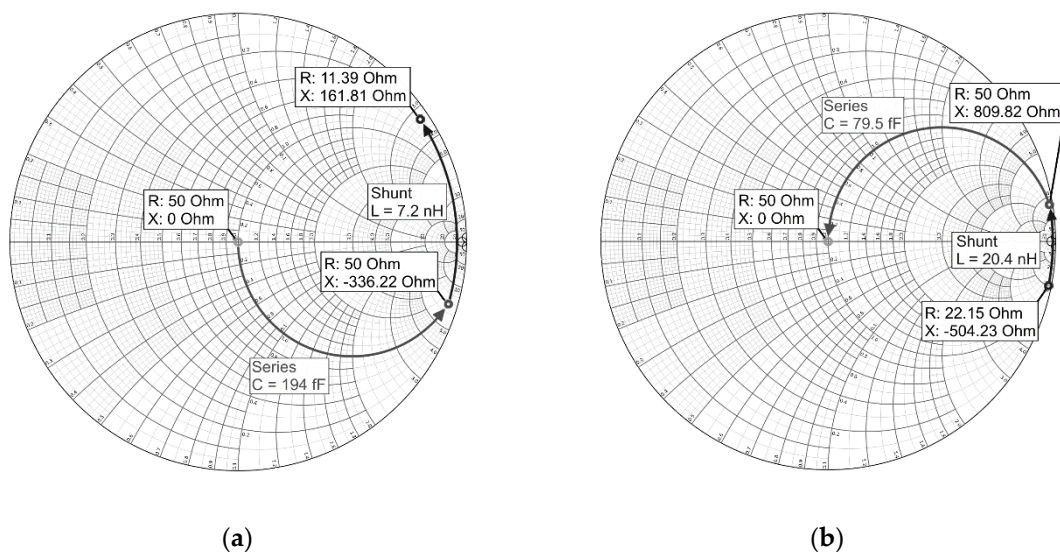
Table 4 summarizes the MOS physical parameters obtained for the maximum gain condition. Using the  $gm/I_D$  design methodology, choosing the M3  $gm/I_D$  ratio of  $10.07 \text{ V}^{-1}$  in order to obtain 700 mV at the M1 gate leads to a  $W/L$  of 20 for the bias network transistor.

**Table 4.** LNA MOS physical design parameters result for maximum gain.

Stage (Transistor)	$gm/I_D$ Ratio [ $\text{V}^{-1}$ ]	$V_{gs}$ [mV]	$V_{gg}$ [mV]	$I_D$ [ $\mu\text{A}$ ]	$W/L$	$L$ [nm]	$W$ [nm]
Common source (M1)	10.07	700	-	3300	1000	65	65,000
Common gate (M2)	12.12	-	1360	3300	3250	65	211,250
Bias network (M3)	11.83	-	-	47.20	20	65	1300

The optimum power gain is obtained from a transistor when  $Y_{IN}$  and  $Y_{OUT}$  are conjugately matched to  $Y_{SOURCE}$  and  $Y_{LOAD}$ , respectively. For an unconditionally stable transistor (or in this case, an unstable one that has been stabilized for the conditions reported in Table 4), it is possible to find a simultaneous conjugate match solution yielding an amplifier design for which the input and output ports are perfectly and simultaneously matched to the load and source. This can be accomplished at any frequency for which S-parameters of a stable transistor are available and provides the maximum stable gain (MSG) at such a frequency. In this case, the conjugate impedance values for the MSG were ascertained as  $(11.39 \Omega + i 161.81 \Omega)$  for the input and  $(22.15 \Omega + i 504.23 \Omega)$  for the output.

Both the input and the output matching networks comprise a series capacitor and a parallel inductor. Figure 15 presents Smith’s chart used for calculating the values of these elements, starting from the conjugate impedance value for the MSG to reach the real  $50 \Omega$  of both the source and the load. The complete LNA schematic circuit, including matching and bias networks, designed for maximum gain condition, is shown in Figure 16.



**Figure 15.** Smith’s chart plot for: (a) LNA input matching network; (b) LNA output matching network.

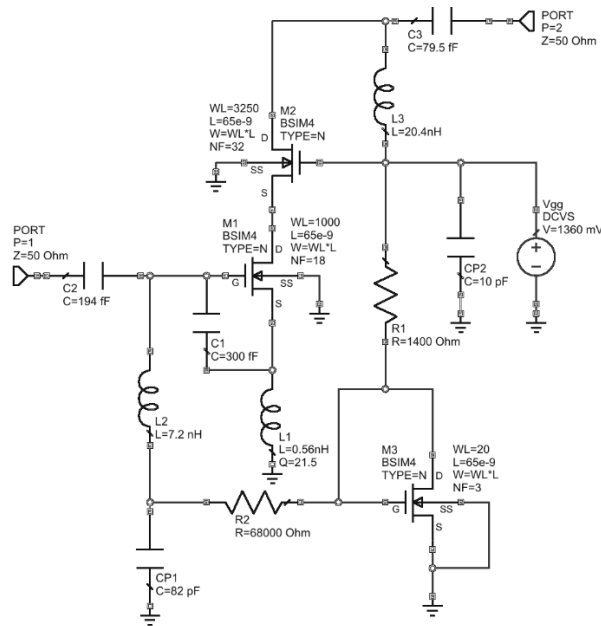


Figure 16. Complete LNA schematic circuit.

The simulation results are presented in Figure 17, where the point of the maximum available power gain of 29.71 dB is located at the working frequency (2.44 GHz) with a noise figure of 0.6257 dB and a K factor of 1.228. It is worth noting that the plot shows a significant gain improvement and noise figure decrease with respect to that reported in the analysis of the cascode stage because the output and the input are now perfectly adapted. This can be verified from the values of  $S_{11}$  (−18.15 dB) and  $S_{22}$  (−30.67 dB) obtained from simulation, reported in Figure 18. Since the K factor is still greater than one, the amplifier maintains its unconditionally stable characteristic.

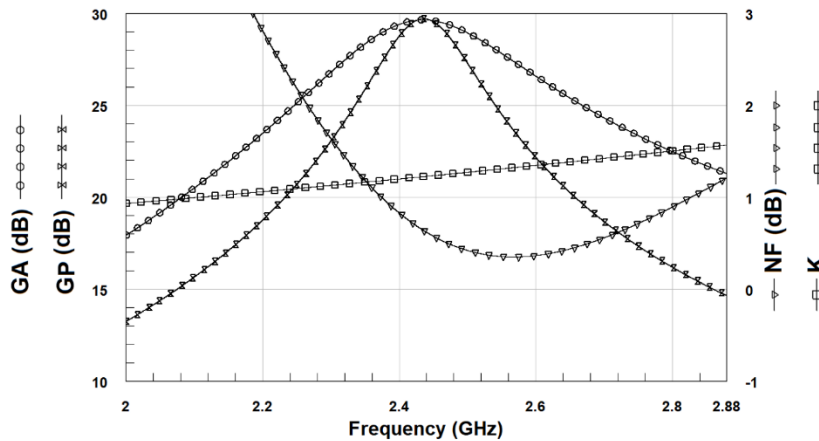
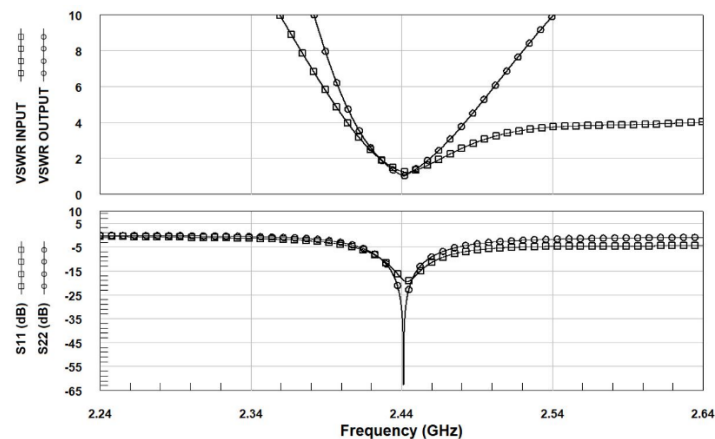


Figure 17. LNA power gain ( $G_p$ ), available power gain ( $G_A$ ), noise figure ( $NF$ ), and stability factor ( $K$ ) (simulation results).



**Figure 18.** LNA input and output return lost ( $S_{11}$  and  $S_{22}$ ), and input and output VSWR (simulation results).

#### 4. Conclusions

This work describes a methodology for designing a cascode LNA combining the use of the S-parameters and the  $gm/I_D$  ratio of each involved MOS transistor. The latter is used as a free variable to explore the design space while allowing designers to optimally bias and size the transistors. It is possible to design the circuit for maximum power gain or for the minimum noise figure, but at the same time, a trade-off can easily be achieved between them. The cascode LNA was chosen as a test vehicle for demonstrating the usefulness of this methodology, and it can also be used with most RF circuit topologies for which the use of S-parameters has been reported for verification purposes only.

The theoretical background behind this methodology was exposed at the beginning of this paper. The link between scattering parameters and the universal  $gm/I_D$  ratio of MOS transistors was demonstrated starting with the hybrid ACM model, whose elements depend on the  $gm/I_D$  of the MOS transistor and using the matrix transformations. However, it is well-known that, especially at high frequencies, S-parameters are more reliably measured than admittance or hybrid parameters. Therefore, looking at more realistic results, designers could directly work with real measured S-parameters as a function of the transistors'  $gm/I_D$  extracted from a test chip, instead of using hand-calculated hybrid parameters and matrix transforms.

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