UMONS
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Faculté Polytechnique

Analog Electronics 2022 Project : Battery Charger

Project Report

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December 2022

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1 Introduction

This project consists in the design and layout of an on-chip constant-current battery charger.

We first calculated the required currents, resistors and operational amplifier (OA) specs of the circuit, and sized the OA transistors using the g_m over I_d methodology. The whole circuit was then simulated using Cadence Spectre, and its efficiency was calculated.

We then did a full layout of the circuit (including the OA) with a 150nm CMOS technology using Cadence Virtuoso and ran DRC (design rules check) and LVS (layout versus schematic) checks. Parasitic extraction and post-layout simulations were performed.

2 Theoretical background

It is usually necessary to use a well-controlled current when recharging a battery. A battery can be modelled by a very large capacitor C in series with a small resistance R_g due to the electrolytes : if a simple voltage source were to be used to charge the battery, a very high initial current would destroy the battery.

It is thus required to limit the charge current. A common solution is to use a constant-current charger. The whole charging circuit that will be used here is displayed on figure 1.

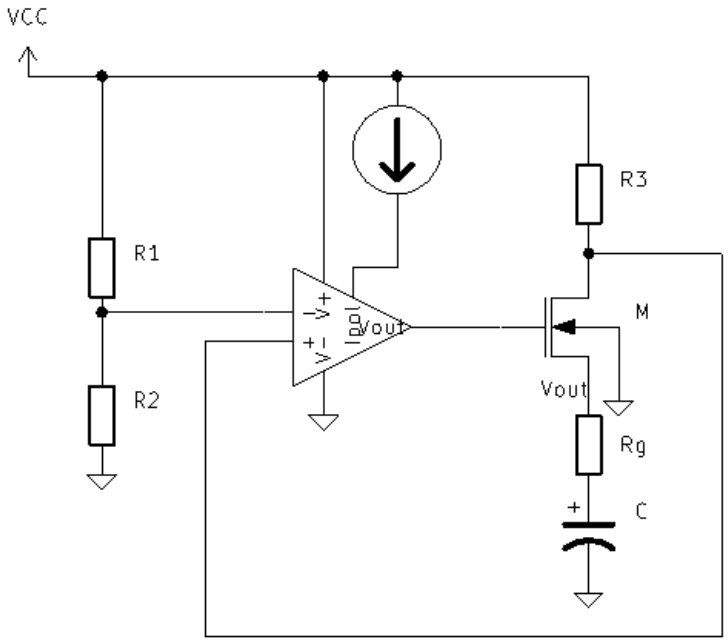


FIGURE 1 – Battery charger circuit

The specs of the battery are the following : 1.2V nominal voltage, 1Ω internal resistance, 30F equivalent capacitance, 10mA maximum charge current, 60minutes charging time. The charger supply voltage is 3.3V.

3 Hand calculations of sizing and biasing

3.1 Currents and resistors

As the OA is connected in negative feedback, we can write (with I the battery current) :

$$V_{cc}\frac{R_2}{R_1+R_2} = V_{cc} - R_3 I$$
$$I = \frac{V_{cc}R_1}{(R_1+R_2)R_3} \tag{1}$$

In order to maximize efficiency, we want to minimize the current going through R_1 and R_2 as it is wasted. We cannot increase the values of these resistors too much however, as the impact of parasitic conductances would become non negligible. We choose arbitrarily to adopt $I_{R_1+R_2} = 100\mu A$. We thus have :

$$I_{R_1+R_2} = \frac{V_cc}{R_1+R_2} \rightarrow R_1+R_2 = \frac{3.3V}{100\mu A} = 33k\Omega \tag{2}$$

We also want to keep the transistor M saturated when conducting $10mA$ in all battery conditions in order for the circuit to work properly. To accomplish this even when the battery is fully charged, we need :

$$I_{R_3} < V_{cc} - V_{out} - V_{DSsat} \tag{3}$$

V_{DSsat} will depend on the transistor size. The smaller V_{DSsat}, the larger the margin for IR_3 but also the larger the transistor size. We choose to use $V_{DSsat} = 0.7V$ (at $I = 10mA$) and $I_{R_3} = 1V$.

$$R_3 = \frac{1V}{10mA} = 100\Omega \tag{4}$$

Now, from (1), (2) and (4), we can calculate R_1 and R_2 :

$$10mA = \frac{3.3VR_1}{33k\Omega 100\Omega} \rightarrow R_1 = 10k\Omega \tag{5}$$

$$R_2 = 33k\Omega - R_1 = 23k\Omega \tag{6}$$

3.2 Sizing of transistor M

We can now size our transistor M, knowing that we chose $V_{DSsat} = 0.7V$ at $I = 10mA$. We are working in saturation and in strong inversion. The current I is given by (with $V_{ov} = V_{GS} - V_{th}$:

$$I = \frac{1}{2\lambda}\mu C_{ox}\frac{W}{L}V_{ov}^2 \tag{7}$$

Knowing that $V_{ov} = \lambda V_{DSsat}$ and that for the technology used $\lambda = 1.2$, we can write :

$$\frac{W}{L} = \frac{2\lambda I}{\mu C_{ox}V_{ov}^2} = 281 \tag{8}$$

Since we want to minimise the transistor area WxL, we choose to use the minimal length allowed by the technology. We thus get $W = 100\mu m$, $L = 0.35\mu m$.

3.3 Calculation of the OA specs in terms of the desired voltages and currents

The operational amplifier that we will use is a differential CMOS amplifier, its schematic can be found on figure 2.

The OA must work with a supply voltage of 3.3V. Additionally, its ouput voltage must be able to vary between $V_{batt_{min}} + V_{ov_M} + V_{th_M}$ (which is unspecified) and $V_{battmax} + V_{ov_M} + V_{th_M} = 1.2V + 0.84V + 0.62V = 2.66V$.

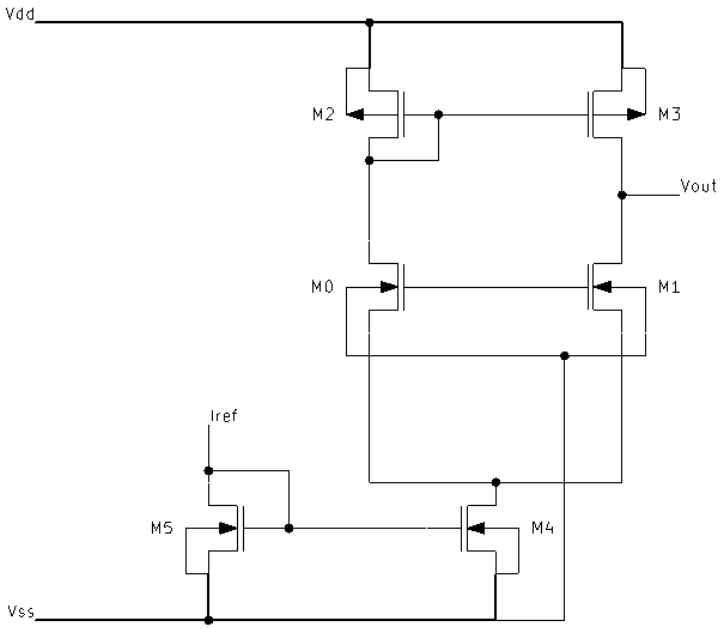


FIGURE 2 – Operational Amplifier

3.4 Sizing and biasing of s OA's transistors with the (gm/Id) methodology

3.4.1 Differential pair

In order to minimize the imbalance in the differential pair due to the OA output current, a bias current much higher than the OA output current is chosen. We choose $I_D = 10\mu A$.

The differential part should work in weak inversion so as to avoid random input voltage offset. However, this would lead to a value of W/L too large. We thus have to work in moderate inversion. We choose $g_m/I_D = 14V^{-1}$. The correspondent current can be found using the technology's g_m over I_d curves (figure 3).

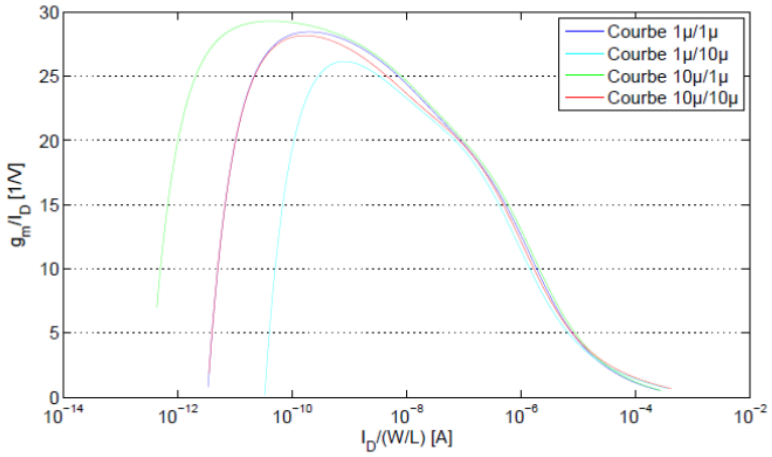


FIGURE 3 – gm/id curve for the nmos

We can see on the figure that for $g_m/I_d = 14V^{-1}$, we get $\frac{I_d}{W/L} = 10^{-6}A$ and thus $W/L = 10$. In order to decrease the Early effect, we choose $L = 1\mu m$ and thus $W = 10\mu$ for M0 and M1.

3.4.2 PMOS current mirror

The PMOS current mirror must work in strong inversion to minimize mismatch errors. So as to allow the OA output voltage to go up to 2.66V, we need $V_{DSsat} < V_{cc} - 2.66V = 0.64V$ for M2 and M3. We choose to use $V_{DSsat} = 0.4V$ to fulfill this condition. We get :

$$\frac{g_m}{I_D} = \frac{2}{V_{ov}} = \frac{2}{\lambda V_{DSsat}} = 4.5V^{-1} \tag{9}$$

The correspondent current can be found using the technology's g_m over I_d curves (figure 4).

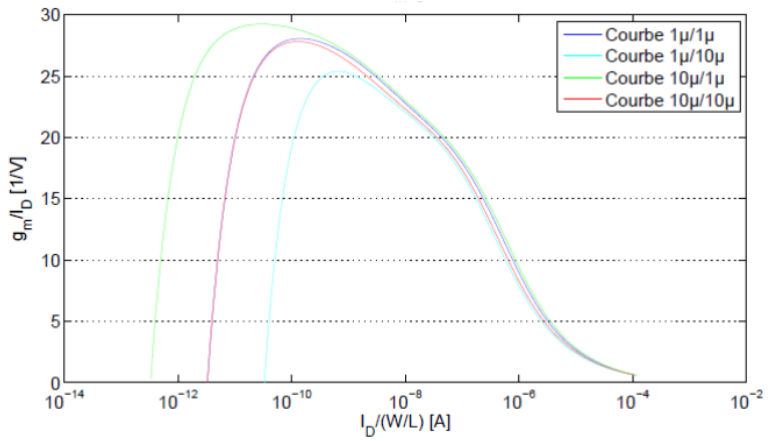


FIGURE 4 – gm/id curve for the pmos

We can see on the figure that for $g_m/I_d = 4.5V^{-1}$, we get $\frac{I_d}{W/L} = 10^{-5}A$ and thus $W/L = 1$. In order to decrease the Early effect, we choose $L = 3.5\mu m$ and thus $W = 3.5\mu$ for M2 and M3.

3.4.3 NMOS current mirror

The transistor M4 has to work in saturation in strong inversion. In order to guarantee saturation, we need :

$$V_{DSsat} < V_{div} - V_{thM1} - V_{ovM1} = 1.52V \tag{10}$$

We choose to use $V_{DSsat} = 1V$. We thus have :

$$\frac{g_m}{I_D} = \frac{2}{V_{ov}} = \frac{2}{\lambda V_{DSsat}} = 1.66V^{-1} \tag{11}$$

The correspondent current can be found using the technology's g_m over I_d curves (figure 3).

We can see on the figure that for $g_m/I_d = 1.66V^{-1}$, we get $\frac{I_d}{W/L} = 10^{-4}A$ and thus $W/L = 0.2$ (as the current through M4 is double the current through M0 and M1). We choose $W = 1.6\mu A$ and $L = 8\mu A$ for M4.

In order to decrease current consumption, we choose to use a current mirror with a gain of 2. We thus have $W = 3.2\mu A$ and $L = 8\mu A$ for M5.

4 Layout

The layout of the battery charger was made using Cadence Virtuoso. We firstly created the OA layout based on its schematic view. We then used the OA cell inside the schematic of the battery charger, and made the charger layout. Finally, we ran several checks as well as parasitic extraction.

The Cadence schematic view of the OA and battery charges are available in annex A.

4.1 Generalities

For both the OA and the charger, the following steps were used during layout :

— **Local placement** : Before making any connections between the elements, we placed the components of each circuit sup-group according to their electrical properties and function so as to minimize circuit imperfections, connections length and chip size.

— **Guard ring generation** : We need a connection to the bulk of the transistor to allow it to work properly by polarizing the substrate. This connection is added to the connections of the drain, the source and the grid. A technique commonly used to connect bulk is to create guard rings. It consists of grouping and surrounding transistors that share the same substrate voltage with the connection to the bulk. This creates a roll-out zone that forms a barrier against the noise that spreads through the substrate. This limits the disturbances of transistors and improves the distribution of bulk voltage. The problem with this technique is that it makes the layout more complex because of the metal layer changes needed to connect the source drain and girdle to other components.

— **Inner routing** : Inner routing involves making connections between components belonging to the same sub-group. The connections are made by metallic "wires" characterized by parasitic effects such as resistances and capacities. It is important to pay attention to the spaces between the tracks of metal belonging to the same layer. Indeed, it is necessary to keep a minimum distance between the different metal tracks to avoid that they interfere with each other. The connections between the different layers are made with vias. Double vias were used in order to minimize imperfections due to resistive effects.

— **Global placement** : Once the sub-groups were ready, they were placed together in a way that tries to minimize inter-group connections length as well as chip area.

— **Outer routing** : Outer routing consists in connecting the different sub-groups as well as the chip input and output pins.

— **Layout verifications** : The first test to verify that the layout is compliant for production is the DRC which stands for Design Rules Check. It checks that the layout respects the geometry and density rules. DRC was run periodically during layout. The second test is LVS which means Layout Versus Schematic. It checks whether the layout corresponds to the reference diagram in terms of electrical components and connections.

4.2 Operational Amplifier

The amplifier is constituted of 3 sub-groups. A PMOS current mirror acting as a charge, a differential pair, to obtain a voltage gain. This pair has a high CMRR to reduce noise at the entrance of the AO and the final sub-group is a PMOS current mirror.

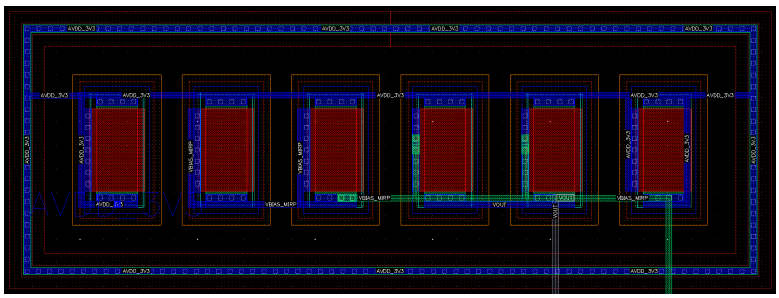
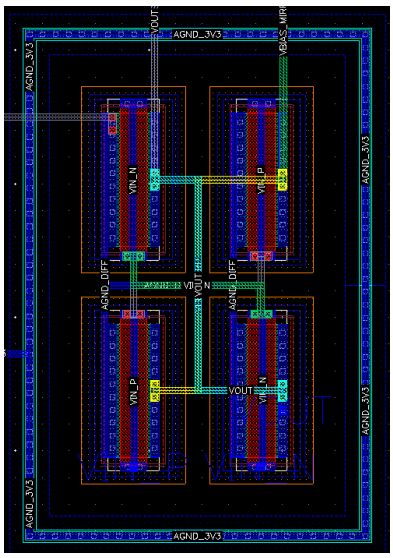


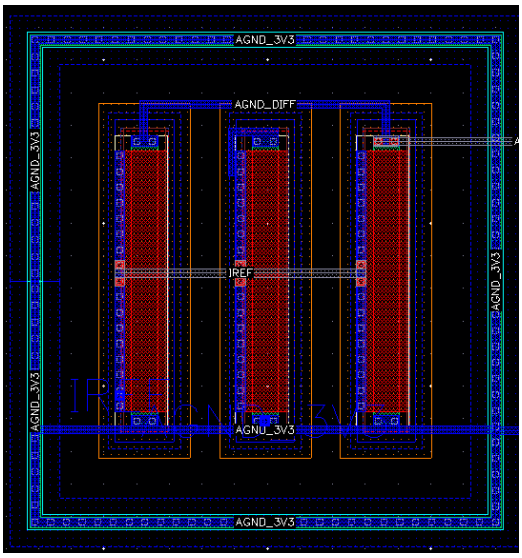
FIGURE 5 – PMOS mirror

In order to make the NMOS current mirror as symmetric as possible, the M5 transistor was split into two even-sized transistors placed on each side of the M4 transistor. Symmetry was

important as it allows to match the parasitic resistors of the current mirror. The NMOS mirror is displayed on figure 6b, with its guard ring.



(a) Differential pair



(b) NMOS mirror

It is also crucial for the PMOS current mirror to be as well-matched as possible. To accomplish this, the PMOS mirror layout was made symmetric, and dummy transistors were used. The dummies help ensure that the active transistors were matched by providing the same surroundings for both of them and reducing mechanical stresses which cause mismatch. The PMOS mirror is displayed on figure 5, with its guard ring.

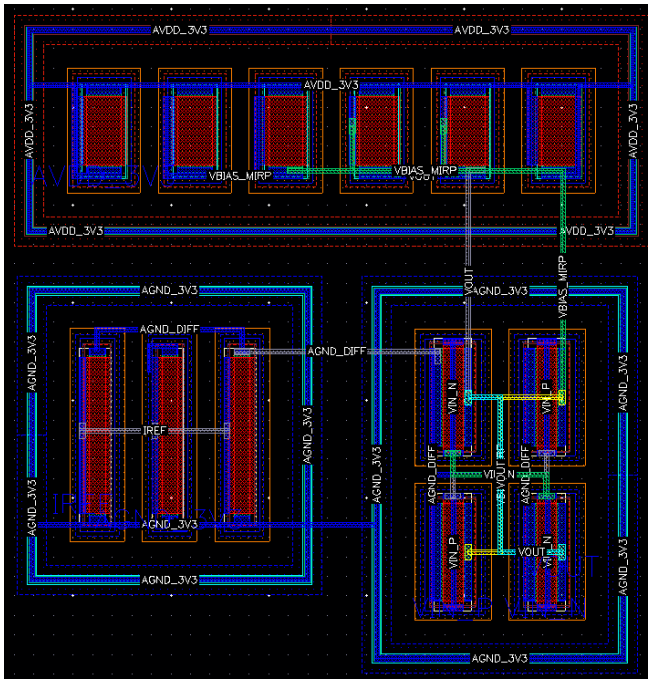


FIGURE 7 – Layout of the OA

Finally, the differential pair is the most critical part of the amplifier in terms of layout, as an improper design will create imperfections such as an offset or common-mode noise effects. For the differential pair, the common-centroid technique was used. Both transistors were split in two, and placed opposite each other diagonally. This technique helps matching the transistors

by minimizing the effects of gradients during manufacturing. The differential pair is displayed on figure 6a, with its guard ring.

Once the layout was complete, DRC was run a last time and returned no errors. LVS was also run and returned no errors either.

4.3 Battery charger

For the charger, real resistors were instantiated. Different types were used for R_1 and R_2 on one hand and for R_3 on the other in order to keep small resistor sizes. Since the length and width of resistors in the layout are quantized, we could not accomplish the exact calculated values. Nevertheless, we got close enough with $R_1 = 9.974\Omega$, $R_2 = 22.99\Omega$ and $R_3 = 100.1\Omega$.

The M1 transistor was split into 10 parts in order to minimize the chip size. The layout of the whole battery charger is diplayed on figure 8.

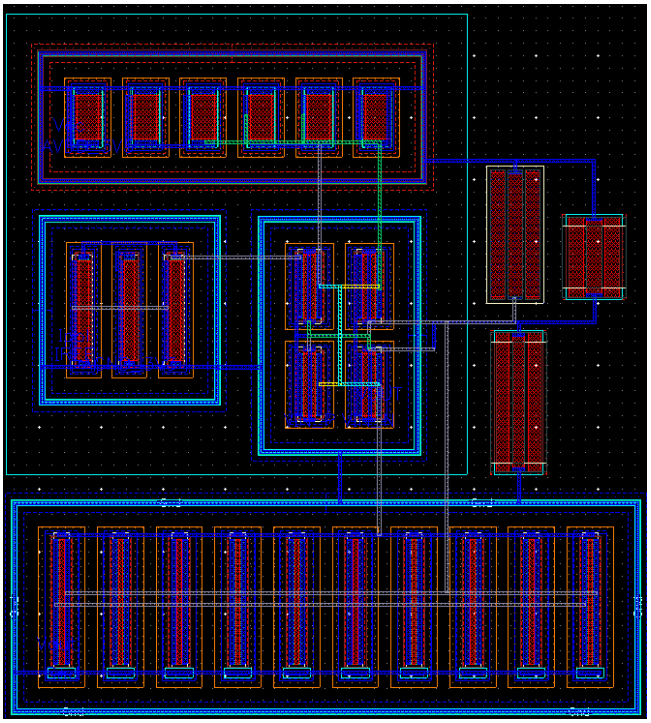


FIGURE 8 – Layout of the whole battery charger

Once the layout was complete, DRC and LVS were run. They returned no error.

4.4 Parasitic extraction

An additional test that can be done is the PEX, which correspond to the Parasitic Extraction of the layout. This consists in calculating the parasitic effects from the physical view in order to perform simulations as faithfully as possible to reality. The routing wires are characterized by a resistivity, resulting in unwanted resistances in the circuits. There is also a dielectric material that separates the different wires, this introduces parasitic capacitive effects. Parasitic inductances are also present in the circuit, though because of their extremely small value due to the small scale of the circuit their effect is negligible in low frequencies.

We ran parasitic extraction for resistances and capacitances. A view of some parasitic resistances is available on figure 9.

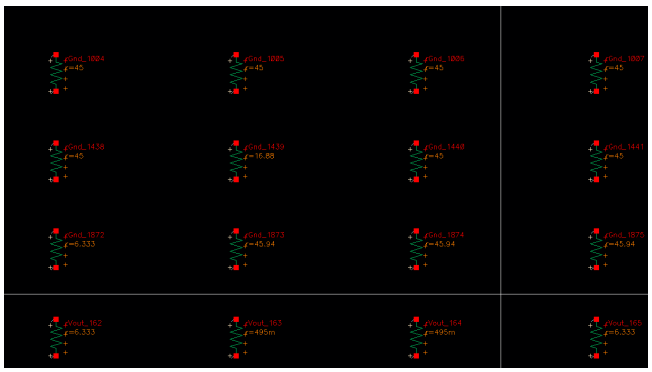


FIGURE 9 – View of some parasitic resistances returned by the PEX tool

5 Simulations using Cadence SPECTRE

5.1 Simulation setup

In order to be able to conduct simulations, we created a Test Bench cell. We instantiated our battery charger as well as a voltage supply, a polarisation current source and an equivalent model of the battery (1Ω resistor in series with 30F capacitor). The schematic view of the test bench is available on figure 10.

Unfortunately, the polarization current source was mistakenly set to $20\mu A$ instead of $10\mu A$, which means the OA performance will not be as good as they could.

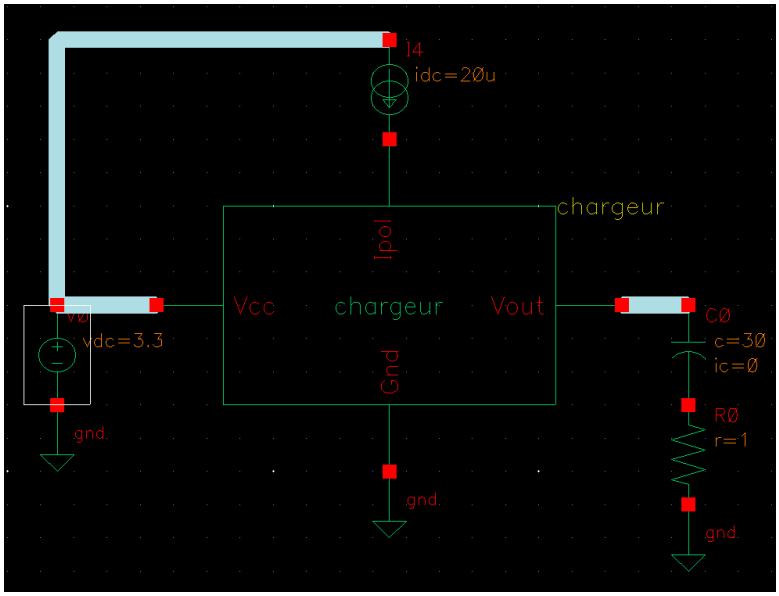


FIGURE 10 – Schematic view of the test bench

Transient simulations from 0 to 4200s were performed for the circuit with nominal supply voltage, +10% and -10% supply voltage, and one additional post-layout simulation taking into account the parasitic extraction with nominal supply voltage.

5.2 Nominal conditions

We obtain the following curves under nominal simulation conditions. These represent the evolution of different circuit parameters as a function of time : V_{div} (red), V_{fbk} (blue), V_{out} (white), the current passing through the load (purple) and the supply current (orange).

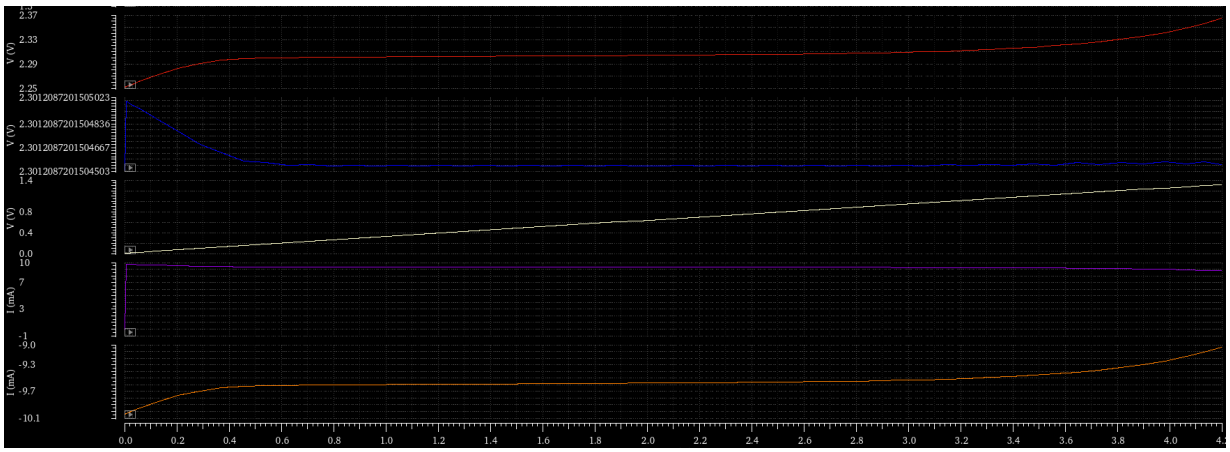


FIGURE 11

There is an initial transient phase after which the values stabilize and a steady state is reached.

We can observe that, V_{fbk} and V_{div}, which are the inputs of the OA have, are almost identical at 2.3V in steady state, though there subsists a small different. We can also see that the current passing through the load is almost constant at about 9.4mA, which is smaller than expected. Supply current is around 9.55mA. Battery voltage increases steadily during the whole simulation, reaching a value of 1.2V after around 3800s, which is a bit slower than expected.

After the battery voltage reaches 1V, an unexpected behaviour is observed in the system. V_{div} rises, while V_{fbk} stats oscillating a bit and the supply current drops. There seems to be a stability problem in the feedback loop.

5.3 Impact of Vcc variations (±10%) on the performances of the circuit

Using a supply voltage of 110% of the nominal voltage, the overall look of the graphs is the same (see annex B). However, there are small changes in currents and voltages. We can see that the time needed to reach the target battery voltage is shorter than at the initial, at 3400s. The steady-state load current is now 10.2mA, with a peak at 11mA during start-up. V_{fbk} and V_{div} are now 10% higher, and V_{fbk} starts oscillating almost from the start of the simulation. Supply current (not represented on the graph) is around 10.4mA.

Using a supply voltage of 90% of the nominal voltage, the behaviour of the system degrades a lot (graphs available in annex B). The time needed to reach the target battery voltage is longer than for nominal conditions, at 4800s (not visible on the graph). The steady-state load current is now 9mA, but it drops very significantly at the end of the charge. V_{fbk} oscillates during the whole simulation, and V_{div} increases at the end of the charge. Supply current (not represented on the graph) is around 9.2mA.

5.4 Post-layout simulation

A post-layout simulation taking into account the parasitic effects with nominal supply voltage was made. The graphs are similar to the circuit in nominal conditions (see annex B). However, there are changes in currents and voltages.

We can see that the time needed to reach the target battery voltage is shorter than at the initial, at 4800s (not visible on the graph). The steady-state load current is now 7.5mA. V_{fbk}

and V_{div} now present a 100mV difference, but there is no more oscillations. Supply current is around 7.7mA.

5.5 Efficiency

The efficiency of the system can be defined as the ratio of the energy provided to the battery (modeled by a capacitor and a resistor) by the energy provided by the power supply.

For the battery energy, we will neglect the series resistor and simply compute the energy stored in the capacitor. For the supply energy, we will neglect the impact of the transient states encountered at the start and end of the simulations and simply multiply the supply voltage by the steady-state supply current by the charge time. [1]

We get :

$$\eta = \frac{\frac{1}{2} \cdot C \cdot V_{out,final}^2}{V_{cc} \cdot I_{supply,s-s} \cdot t_{charge}} \tag{12}$$

For the theoritical circuit the supply current is the sum of the current in three branches : the load, the resistive divider and the polarization current source.

$$\eta = \frac{\frac{1}{2} \cdot 30F \cdot (1.2V)^2}{3.3V \cdot (10mA + 0.1mA + 10\mu A) \cdot 3600s} = 0.180 \tag{13}$$

For the simulations, the values of the supply current and charge time mentioned in the previous subsection were used for efficiency calculation.

6 Comparison between calculated values and simulations results

Value	Calculated	S. Nominal	S. Low V_{cc}	S. High V_{cc}	Post-layout
I_{bat} [m A]	10	9.4	9	10.2	7.5
Charge time [s]	3600	3800	4800	3400	4800
Efficiency	0.180	0.180	0.148	0.185	0.177

TABLE 1 – Comparison of values

7 Conclusion

In this project, we designed an on-chip constant-current battery charger.

Firstly, we calculated the necessary currents and resistances for the circuit and we sized the operational amplifier (OA) using the g_m over I_d methodology. Once all these specifications were calculated, the circuit was simulated using Cadence Spectre and its efficiency was calculated.

We then focused on the layout part. We used a 150nm CMOS technology with the help of Cadence Virtuoso. And performed local and global placement, guard ring generation, inner routing and layout verifications using DRC and VLS. Once the layout was finished, we were able to test the impact of a V_{CC} variation ($\pm 10\%$) on the circuit performances and calculate its efficiency.

1. More rigorously, one should use the integral of the supply current over time and consider the fact that the resistive losses in the battery are a measure of the battery efficiency not the charger efficiency.

As a bonus, we performed parasitic extraction and post-layout simulations, which allowed us to observe the impact of parasitic effects on the circuit.

The different results obtained have been summarised in section 6.

A Schematics

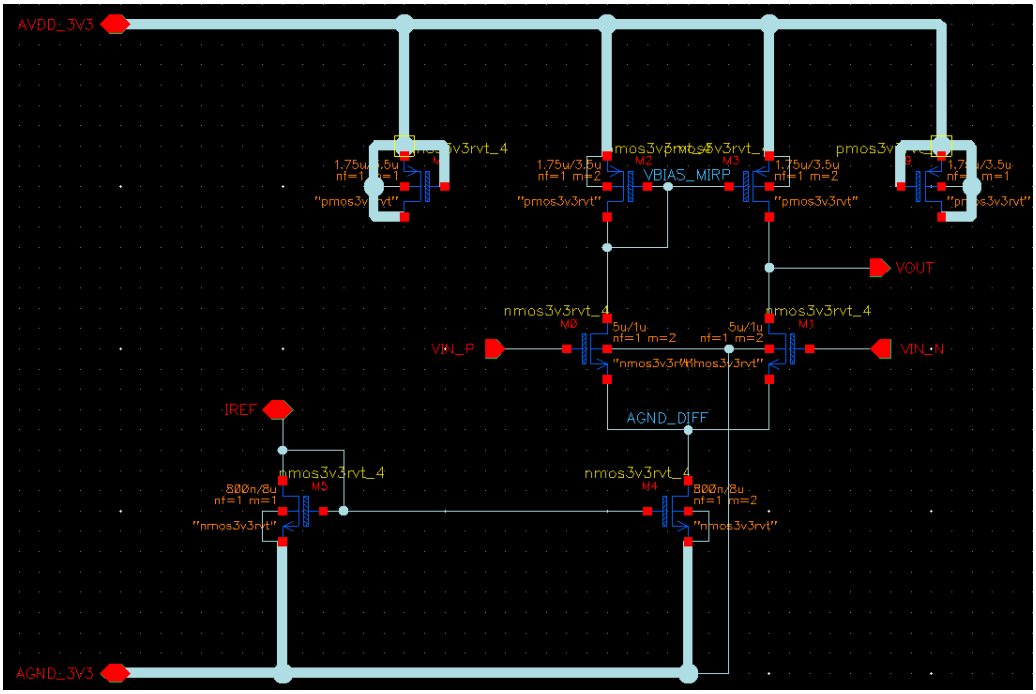


FIGURE 12 – Cadence schematic view of the OA

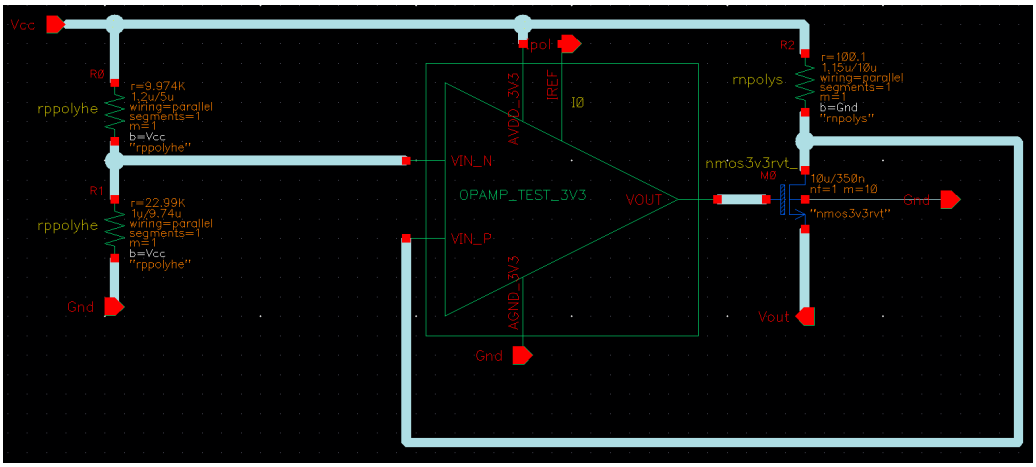


FIGURE 13 – Cadence schematic view of the charger

B Simulations

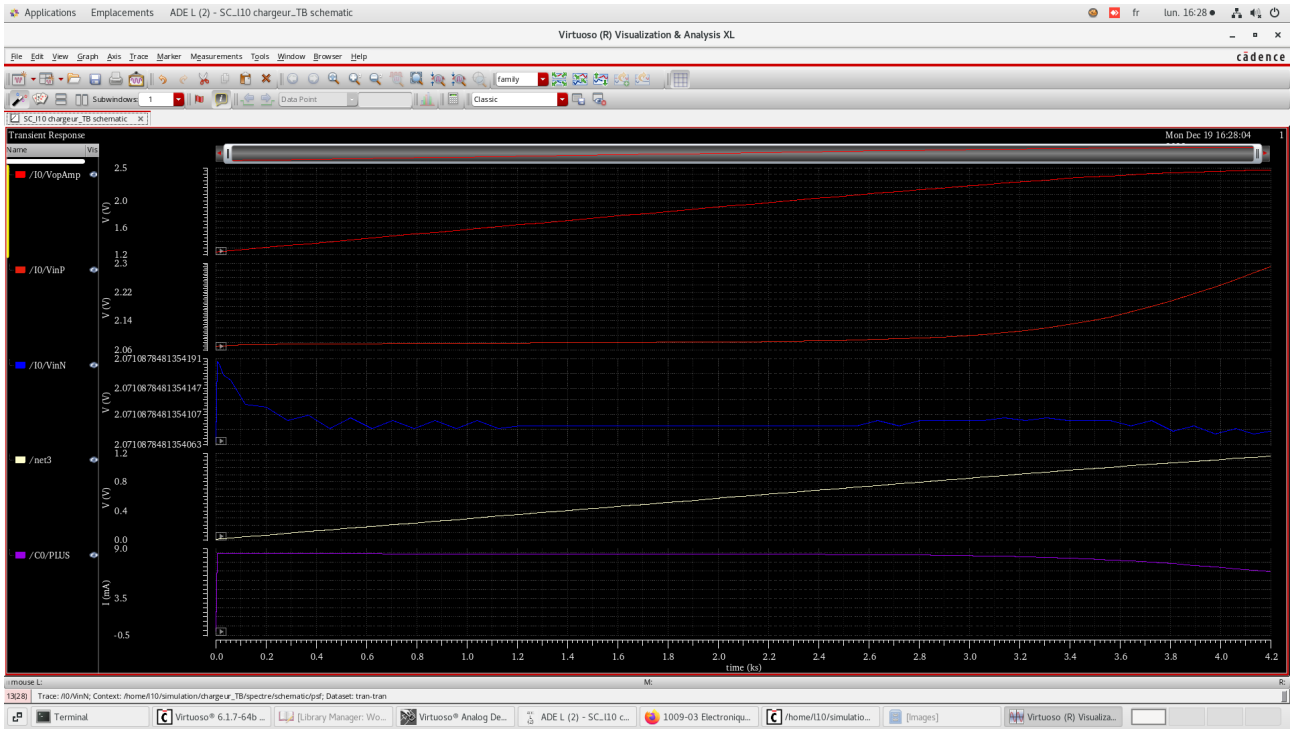


FIGURE 14 – Simulation results for 90% VCC and without considering PEX

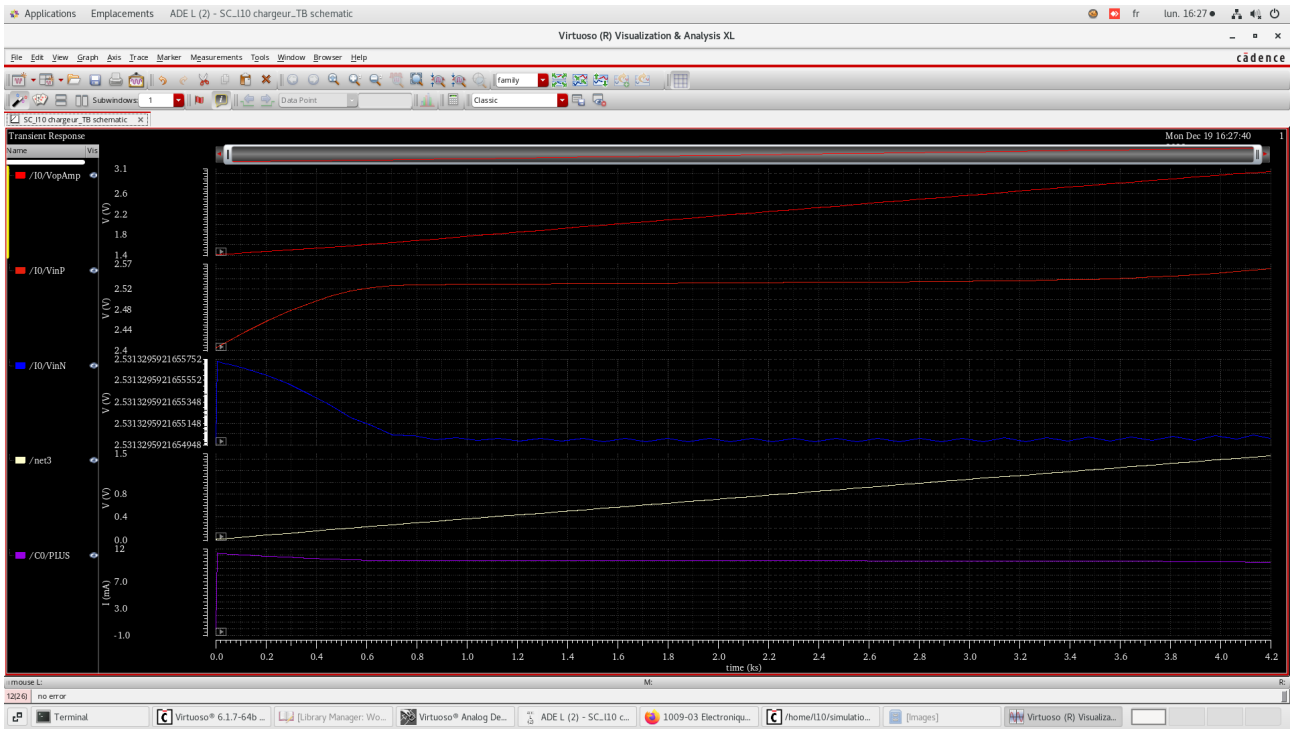


FIGURE 15 – Simulation results for 110% VCC and Without considering PEX

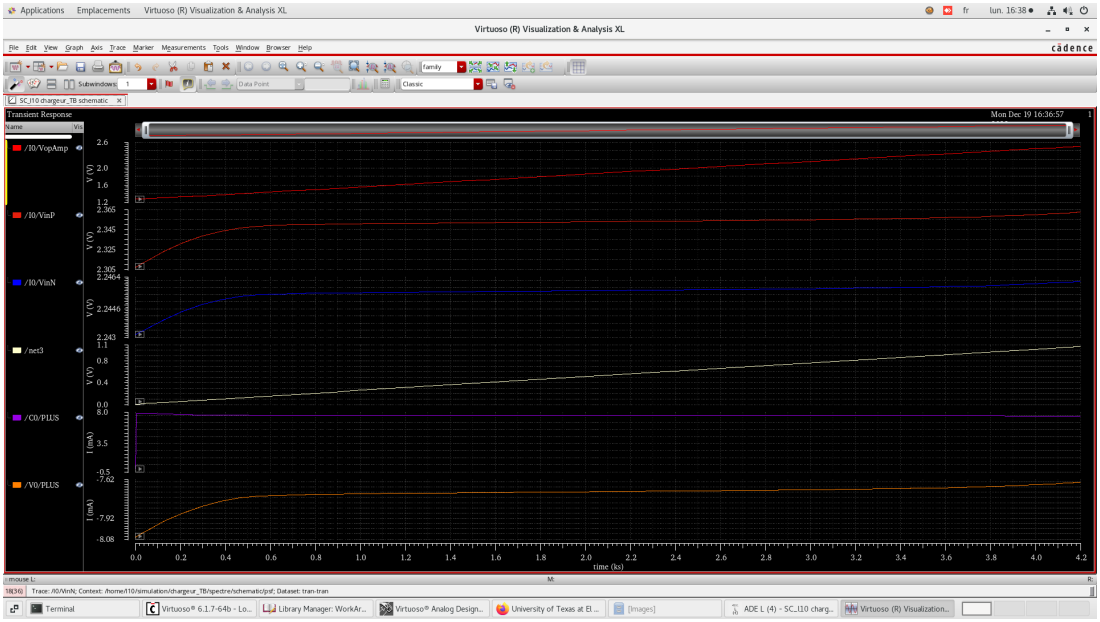


FIGURE 16 – Simulation results with parasitic extraction