IEEE Open Journal of
Circuits and Systems

Received 27 September 2022; revised 17 December 2022; accepted 17 December 2022. Date of publication 28 December 2022;
date of current version 2 March 2023.

Digital Object Identifier 10.1109/OJCAS.2022.3232638

Influence of PVT Variation and Threshold Selection on OBT and OBIST Fault Detection in RFCMOS Amplifiers

HENDRIK P. NEL [1], FORTUNATO CARLOS DUALIBE [2] (Senior Member, IEEE), AND TINUS STANDER [1] (Senior Member, IEEE)

[1]Department for Electrical, Electronic and Computer Engineering, Carl and Emily Fuchs Institute for Microelectronics, University of Pretoria, Pretoria 0002, South Africa

[2]Electronics and Microelectronics Department, Polytechnic Faculty, Université de Mons, 7000 Mons, Belgium

This article was recommended by Associate Editor C.-M. Hung.

CORRESPONDING AUTHOR: H. P. NEL (e-mail: u12077497@tuks.co.za)

This work was supported by the NRF/F.RS.-FNRS South Africa–Wallonia Joint Science and Technology Research Collaboration under Grant UID107864, as well as NRF Grant UID137950.

ABSTRACT Oscillation-based testing (OBT) and Oscillation-based built-in self-testing (OBIST) circuits enable detection of catastrophic faults in analogue and RF circuits, but both are sensitive to process, voltage and temperature (PVT) variation. This paper investigates 15 OBT and OBIST feature extraction strategies, and four approaches to threshold selection, by calculating figure-of-merit (FoM) across PVT variation. This is done using a 2.4 GHz LNA in 0.35 μm CMOS as DUT. Of the 15 feature extraction approaches, the OBT approaches are found more effective, with some benefit gained from switched-state detection. Of the four approaches to threshold selection (nominal-ranged static thresholds, extreme-range static thresholds, temperature dynamic thresholds, and simple noise-filtered tone detection), dynamic thresholds resulted in the highest average FoM of 0.919, with the best FoM of 0.952, with a corresponding probability of test escape $P(T_E)$ and yield loss $P(Y_L)$ of $5{\cdot}10^{-2}$ and $1.89{\cdot}10^{-2}$ respectively but requires accurate temperature measurement. Extreme static threshold selection resulted in a comparable average FoM of 0.912, but with less susceptibility to process variation and without the need for temperature measurement. Binary detection of a noise-filtered oscillating tone is found the least complex approach, with an average FoM of 0.891.

INDEX TERMS Built-in self-test, circuit simulation, CMOS, design for testability, LNA, microwave integrated circuits, oscillation-based testing, PVT.

I. INTRODUCTION

WITH the increased application of RF front-ends in system-on-chip (SoC) devices, the need to characterize RF components with very few accessible nodes has become a challenge both in terms of cost and ease of testing [1]. Analogue and RF components need accessible nodes in order to be tested with traditional or automated methods that occupy valuable chip space and introduce additional probe-pad parasitics [2]. Several design-for-test (DfT) strategies can reduce test time and complexity, with most being defect-oriented to detect or diagnose failures [3]. Such strategies include, but are not limited to, process-control monitors (PCM), current monitoring, envelope monitoring, oscillation-based testing and on-chip stimulus generation [4], [5].

Numerous approaches to analogue [6], [7], [8] and RF [9], [10], [11], [12], [13], [14], [15] built-in self-testing (BIST) have been proposed, with most of the state-of-the-art techniques relying on indirect parameter measurement using nonintrusive sensors [16] or predictive modelling [17], whereas the classical approaches [18] require the application of some test stimulus.

One technique to reduce test complexity and achieve high fault coverage is through oscillation-based-testing

(OBT) [19], [20], [21], [22], [23], [24], [25] and oscillation-based built-in-self-testing (OBIST) [6], [25], [26] circuits, with the distinction illustrated in Fig. 2.

In both OBT and OBIST circuits, the circuit under test (CUT) is connected into an astable feedback loop to convert the CUT into an oscillator [27]. The feedback loop required to establish natural oscillation may be passive if the CUT has gain, but gain may be introduced if the CUT is passive or has low gain. Deviation from the nominal behaviour of the oscillator can then be used to detect or diagnose faults in the CUT.

OBT and OBIST have been applied to a wide variety of analogue and mixed-signal (AMS) CMOS circuits, including operational transimpedance amplifiers (OTAs) [28], [29] and OTA-based filters [30], second-generation current conveyors (CCIIs) [31] and CCII-based filters [32], conventional op-amps [33], switched capacitor filters [34], [35], digital circuits such as digital filters [36], full AMS blocks [37] and phase shifters [38].

OBT uses test equipment to measure the oscillation parameters [25], [27], and may also be used to establish the feedback loop [29]. At RF frequencies, these instruments typically only measure scalar values of frequency and power [38], but at least one RF node needs to be accessed off-chip in the case of RF OBT CMOS testing.

OBIST, in contrast, incorporates all of the testing circuitry on-chip (including switches to switch the CUT from its nominal system integration into an OBIST test mode), with no need for RF test equipment or off-chip RF interfaces [39], [40]. Apart from the time and cost saving in production testing, this further enables in situ testing during deployment. The drawback of OBIST is, however, that the test circuitry is subject to the same process, supply voltage and temperature (PVT) variation as the CUT; a problem which has been discussed in the context of other RF BIST approaches [41], [42], [43], [44], [45], but has not received much attention in OBT and OBIST literature [45]. Adaptive test strategies may be used to dynamically alter test parameters based on wafer or die properties [46], [47], [48], [49], [50], including at RF [51], and should be considered in an OBT test threshold selection evaluation. Temperature-aware adaptive testing has also been shown to improve test efficacy [49], [52], especially when combined in full PVT awareness [53] but has not been explored in an OBT or OBIST context for RFCMOS.

This paper presents an extensive study on the impact of test feature extraction, and threshold selection, on both OBT and OBIST under PVT variation at RF, using a 2.4 GHz LNA in 0.35 μm CMOS [40] as CUT, operating from a nominal V_{DD} of 3.3 V. The process is selected for its low prototyping cost and prior usage for demonstrating novel RF circuit principles [54], [55], [56], [57]. This work extends on [40] by considering full PVT variation and not only process variation, comparing 15 OBT and OBIST approaches (as opposed to the original four), improving on the definition of the OBT figure-of-merit (FoM) and relating it to the more commonly used Test Escape (T_E) and Yield Loss (Y_L) parameters. To the authors' knowledge, this is the first study of OBT and OBIST in RFCMOS.

A critical consideration addressed here is the selection of detection thresholds and comparing different approaches to setting thresholds under PVT variation. We further present more details on the design and response of critical power detectors, data to motivate the choice of Johnson SB distributions in fitting, and explicit distinctions between OBT and OBIST test approaches. This investigation into RF OBT and RF OBIST threshold selection and resulting efficacy, when faced with PVT variation, is an important step toward commercial adoption of the techniques.

The paper is organized as follows:

Section II presents the circuit under test (CUT) and its nominal performance, derived largely from our prior work in [40]. Section III discusses the fault modeling and simulation setup of the circuit, with Section IV describing the postprocessing of the data generated in simulation. Section V presents the different threshold selection approaches. Section VI presents the results of the study with some discussion, and the study is concluded in Section VII with a summary and avenues for future inquiry.

II. CIRCUIT DESIGN AND NOMINAL OBT/ OBIST DATA

The full test circuit [40] is shown in Fig. 1. The CUT is a 2.4 GHz LNA using a popular two-stage common-source topology (M_3-M_4), with inductive source degeneration L_s in the first stage. The OBT switching and feedback circuitry ($M_{1,2,5,6}$, $C_{FB,ST}$, $L_{1\text{-}3}$) is designed to form part of the LNA matching network, which was a key contribution of our prior work in [40]. The LNA achieves above 10 dB gain and below 4 dB NF from 1.25 – 2.6 GHz during nominal operation, which compares favourably with 12 dB gain and 3.4 dB NF without the switching components (Fig. 3).

The feedback path has a switchable shunt capacitor (C_{ST}) to ground, which alters the gain and phase shift of the feedback loop and, consequently, generates two distinct and selectable OBT oscillation frequencies. Subsequent analyses will show that this measure can improve the fault identification and FoM of certain OBT strategies.

The RF power detector uses a single NMOS transistor in common-gate configuration, matched with coupling capacitor C_{CPD} and inductor L_{PD} in series to a DC load R_0. R_2 provides a high resistance path to ground for the power detector. The loading effect of the detector is minimised by utilising a −10.35 dB resistive power-divider M_8-R_1 which maintains a low insertion loss of less than 2.12 dB. The LC matching circuit results in a frequency-dependent DC output voltage that decreases linearly from 0.5–2GHz at nominal temperature (Fig. 4). This enables separate frequency and output power discrimination by power detection alone, when used in conjunction with two switched oscillation states at different frequencies.

The RF power detector, outlined in red in Fig. 1 (M_8-M_9, R_0-R_2, L_{PD} and $C_{CPD,PD}$), is considered part of the

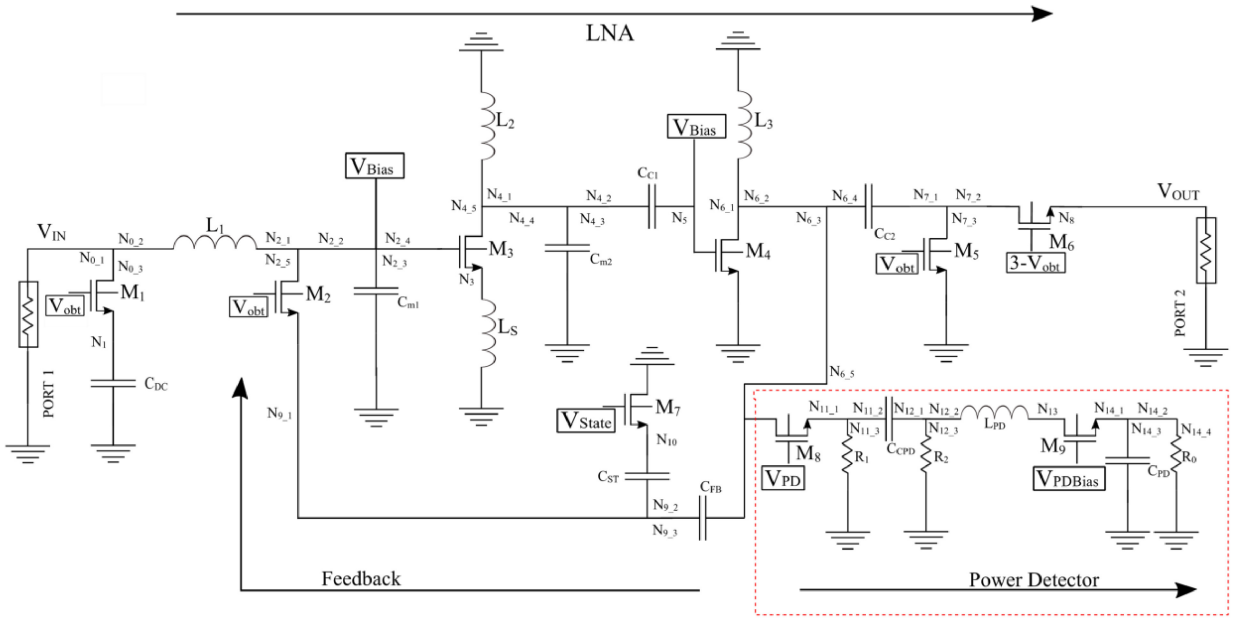


FIGURE 1. Full LNA, feedback and power detector circuit schematic. The power detector, outlined in red, is included in OBIST simulations but excluded in OBT simulation.

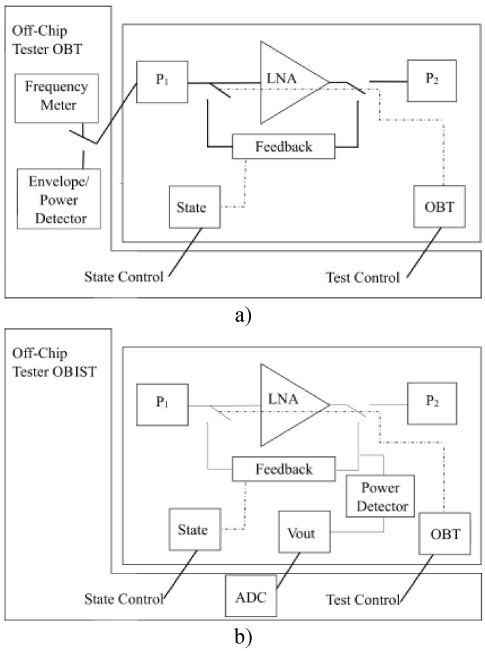


FIGURE 2. Test interface for a) OBT circuit and b) OBIST circuit.

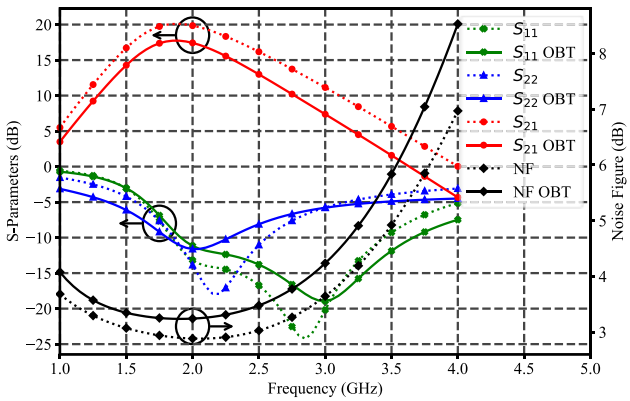


FIGURE 3. LNA NF and S-Parameters, with and without OBT circuitry.

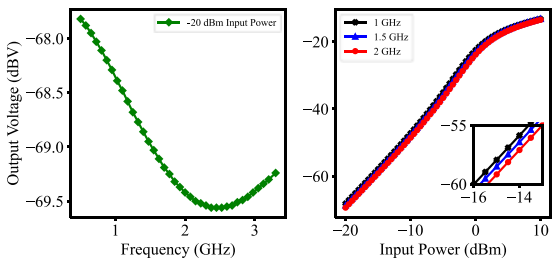


FIGURE 4. Power Detector frequency response (left) and sensitivity (right).

OBIST circuit when faults are simulated and the FoM is calculated, and the voltage at node N_{14} monitored. For OBT evaluation (where off-chip RF detection is assumed), the RF power detector circuit is excluded from fault injection and FoM calculation. For OBT evaluation, the voltage of the fundamental and three harmonics, as shown in Fig. 6, at node N_{0_1} (Port 1) are monitored and converted to power using an ideal power detector and filter as would be the case for off-chip OBT detection (Fig. 2).

It is important to note the temperature dependence of the on-chip power detector used in OBIST testing, as shown in Fig. 5. The mean of the output is decreases over frequency for the different temperatures but increases on average with temperature. It is further of note that the standard deviation of the output decreases with an increase in temperature, as the deviation at higher temperatures are dominated by the temperature of the device and not the noise variation at the input. This is shown later in the paper to manifest in the performance of OBIST circuits.

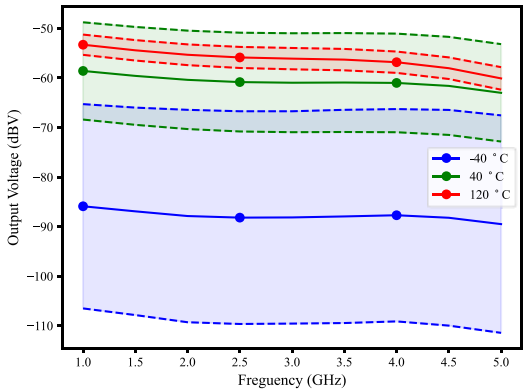


FIGURE 5. Power Detector frequency response for temperature and process variation at −20dBm input power. Solid lines indicates the mean and the dashed lines indicating one standard deviation from the mean.

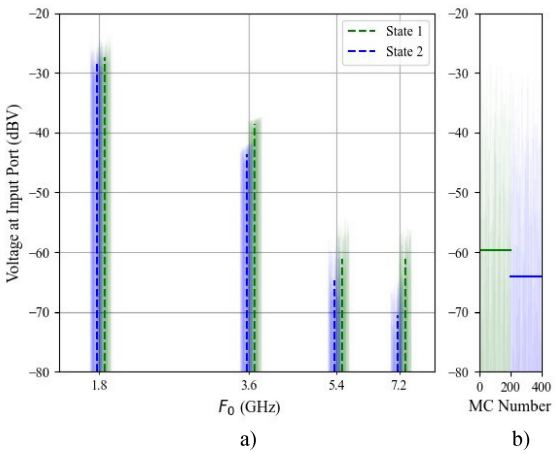


FIGURE 6. Nominal outputs for a) fundamental and three harmonics of the oscillator at Port 1 (OBT) and b) DC value output of the total power detector at node 14 (OBIST).

The nominal output of the voltage at Port 1 in both states of the OBT circuit is plotted for the fundamental and three harmonics in Fig. 6 (a). The nominal DC output of the power detector, of the OBIST circuit, at node N_{14} in both states is shown in Fig. 6 (b). Solid lines represent the nominal values, whereas faded lines show the results over 200 Monte Carlo (MC) analyses.

III. FAULT MODELLING AND SIMULATION SETUP

A. FAULT MODELLING

The most common way of evaluating OBT circuits is by evaluating them over single-catastrophic or single-deviation fault models [19], [20], [21], [26], [27], [31], [40], enabling the use of fault coverage to evaluate the efficacy of the testing strategy. This is often augmented by Monte Carlo analysis of both faulty and non-faulty circuits [58] to evaluate the test approach over PVT variation. In this work, only single-catastrophic faults are considered, as the consideration of parametric faults [30] increases the number of required simulations substantially.

Each fault-injected circuit is evaluated over a range of PVT variation. Open-circuit (OC) and short-circuit (SC) faults are considered, with OC faults modelled with a 1 MΩ resistor (replacing the conducting node) and SC faults modelled with a 10 Ω resistor between two nodes. This matches the approach used previously [19], [27], [31], [40], with the only difference being the choice of 1 MΩ resistor for the OC, as opposed to 10 MΩ previously, to ensure correspondence to the previous paper [40]. Based on the results in [31], this change is not expected to influence the test results.

OC faults are connected in the redundant branches and are chosen based on the layout of the device. These redundant branches can be seen in Fig. 1 as N_{A_B}, where A is the node number and B the redundant branch (e.g., N_{4_3} is the third redundant branch in node 4). This gives an OC fault count of 41 possible faults. For SC faults, $N \times (N-1)/2$ non-redundant short-circuits are possible between N nodes, leading to a total of 120 fault cases for 16 nodes (N0-N14, with N15 as ground). The total faults in the circuit for the OBIST circuit (including the power detector) is 161, and for the OBT circuit 146 (without the power detector).

The number of faults simulated under PVT and MC is reduced to a manageable dataset of 30 faults 19 OC and 11 SC) that oscillate, by assuming that the circuit will not oscillate under any other PVT condition if it does not oscillate at nominal PVT. Of these 30 faults that exhibit oscillation under nominal conditions, 15 manifests in the power detector, while the other 15 occur in the main LNA. It is further important to note that the oscillation condition of the CUT is minimally affected by faults in the on-chip power detector in case of OBIST testing, because of the minimal loading of the power detector on the oscillating circuit; however, the OBIST circuit's ability to detect these oscillations may be impeded by a faulty power detector. For this reason, faults in the power detector are considered as a faulty CUT if the OBIST circuit.

B. SIMULATION SETUP AND DATA RECORDING

A Periodic Steady State (PSS) simulation is used for each schematic setup to determine the frequency and power of oscillation harmonics from 600 MHz to 2.6 GHz, with a 200 run Monte Carlo (MC) analysis for each netlist. The PDK's standard sensitivity parameters are used, introducing variation both to active and passive circuit components.

Both switched oscillation states are simulated (state 1 with $V_{\text{state}} = 0$ V, and state 2 with $V_{\text{state}} = 3$ V), with the two complementary runs using the same starting seed for the MC run. Both OBT and OBIST data are considered. For OBIST detection, only the voltage output at the power detector for each state are recorded at each simulation, as depicted in the test OBIST interface Fig. 2 (b).

To evaluate OBT testing (i.e., evaluating test efficacy under the assumption that frequency and power measurements are available off-chip), only the detected voltage (first four harmonics) output at the input port and fundamental frequency is recorded, as depicted in the OBT test interface in Fig. 2 (a).

From the recorded data for the OBIST and OBT circuit, 9 strategies for output data recording are considered. These are:

OBIST:

1. P_1 (dBV), the power detector (PD) DC output for the oscillator in state 1.
2. P_2 (dBV), the PD DC output in state 2.
3. $|P_1 - P_2|$ (dBV).

Power detected OBT:

4. P_{1OBT}, the port 1 total power in oscillating state 1 (dBm). OBT equivalent of Strategy 1.
5. P_{2OBT}, the port 1 total power in oscillating state 2 (dBm). OBT equivalent of Strategy 2.
6. $|P_{1OBT} - P_{2OBT}|$ (dBm). OBT equivalent of Strategy 3.
7. P_{LPF1} (dBm), the port 1 total power in oscillating state 1, frequency-filtered on a -20 dB/decade slope, producing an output power proportional to frequency. OBT equivalent of Strategy 1 with frequency dependence.
8. P_{LPF2} (dBm), the port 1 total power in oscillating state 2, frequency-filtered on a -20 dB/decade slope, producing an output power proportional to frequency. Frequency dependent OBT equivalent of Strategy 2.
9. $|P_{LPF1} - P_{LPF2}|$ (dBm). Frequency dependent OBT equivalent of Strategy 3.
10. $|P_{1OBT} - P_{LPF1}|$ (dBm) the difference of port 1 total power in oscillating state 1 (dBm), directly and through a low pass filter.

Voltage and frequency OBT:

11. V_1, the port 1 voltage at fundamental oscillating tone in state 1 (dBV).
12. V_2, the port 1 voltage at fundamental oscillating tone in state 2 (dBV).
13. $|V_2 - V_1|$, where V_2 is the port voltage in state 2 (dBV).
14. Frequency of fundamental oscillation tone in state 1 (f_1).
15. $|f_2 - f_1|$, where f_2 is the frequency of fundamental oscillation tone in state 2.

All test results are interpreted in terms of analog voltage values, neglecting possible effects of finite ADC resolution or comparator offset error.

C. PARAMETRIC SWEEP PROCEDURE

The full flow of the simulation is shown in the flow chart in Fig. 7, including parametric sweeps in voltage from 2.805 to 3.795 V in 0.165 V increments, and temperature variation from −40 to 160∘C in 10 °C increments. The prior described MC analysis is repeated at each unique voltage and temperature increment to simulate process variation.

This simulation flow leads to the following assumptions:

1. If the circuit with an injected fault does not oscillate at nominal voltage and temperature at the TT corner in both state 1 and state 2, it is assumed that it will not oscillate at other temperatures, voltages or process values for the same injected fault. These faults are considered 100% detectable.
2. If one of the circuit simulation MC points fails for a specific sample of temperature and voltage, it is assumed that the circuit outputs will be the same as the nominal circuit (i.e., without OBT/OBIST switches engaged). In these cases, the port data for the nominal PSS simulation at the current temperature, voltage and MC point is applied as detected quantities.
3. The sequence of process variations over 200 iterations of the MC analysis will be the same if the same seed value is selected. This means that MC analysis may be applied sequentially to state 1 and state 2 operation, with identical process variation considered, emulating the same manufactured circuit.

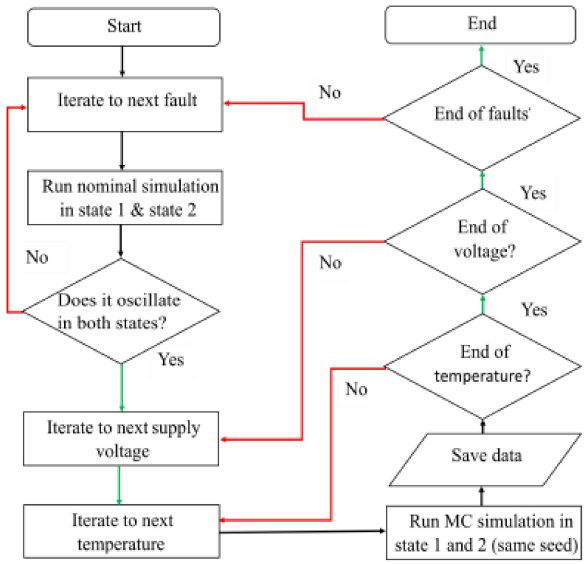


FIGURE 7. Simulation flow chart.

IV. DATA POST-PROCESSING

The simulation flow in Section III produced 48 data features from 8820 distinct, 200-point MC simulations of process variation (1,764,000 simulations in total), iterating through 30 faults, 21 temperature points, 7 supply voltage values and 2 states. To interpret the data, the data post-processing flow in Fig. 8 is followed.

We present data in various stages of processing throughout the paper. An example of the lowest level of processing is shown in Fig. 10, presenting a single Monte Carlo process variation run, for a specific fault at a specific temperature and supply rail value, using a specific detection strategy (Strategy 1). This data is reduced, for a specific test strategy, by fitting the distribution pictured in Fig. 10, aggregating these results over all injected faults to calculate the FoM as per Equation (12), and then repeated for incremented voltage and temperature values. These results are then consolidated on a heatmap (one for each test strategy) as presented in, e.g.,

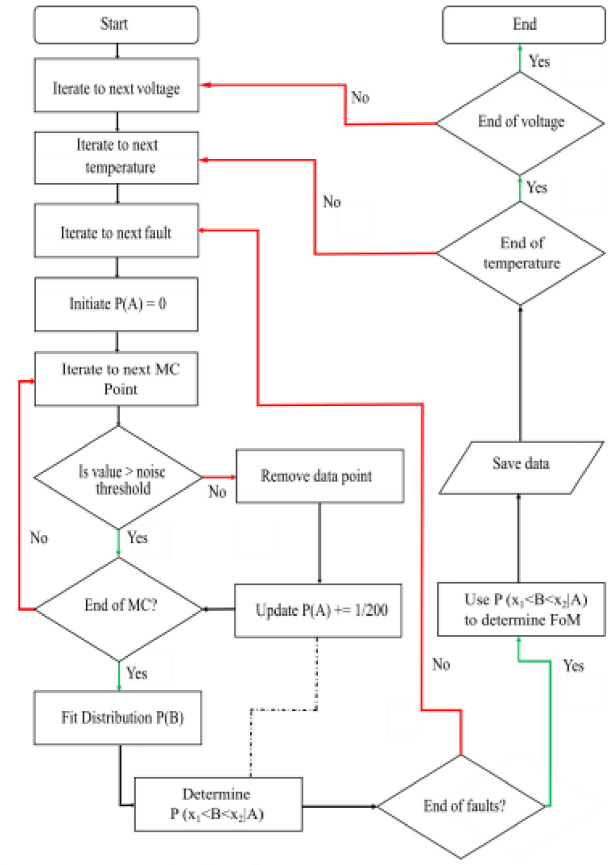


FIGURE 8. Data processing flow chart.

Fig. 16. Finally, the data in the heat maps are consolidated into box plots and compared side-by-side in Fig. 23-Fig. 25.

This procedure reduces the features of each simulation to a 2D array of FoM values that is dependent on supply voltage and temperature. For all the fault simulations associated with a specific supply voltage and temperature, all the feature data are noise-threshold filtered before the data is fitted to distributions and the number of threshold-filtered data points counted. The distribution mean and variance for the data above the detection threshold, as well as the number of data points below the detection threshold, are then used to determine the probability for each fault to lie within the detection thresholds of the nominal working circuit. After all the probabilities for all the faults are determined and scaled, these are used to determine the FoM of the test procedure for that specific voltage and temperature (VT) point. This is then iterated over all supply voltages and temperatures.

A. PROBABILITY CALCULATION AND THRESHOLD APPLICATION

The probability that a random variable lies between two detection thresholds x_1 and x_2, i.e., $P(x_1 < X < x_2)$ (where X may be detected power, frequency or voltage, or a combination of quantities, as outlined in the 15 strategies previously) is key to evaluating the FoM of an OBT or OBIST strategy. Our approach to PDF fitting and detection probability calculation is outlined here.

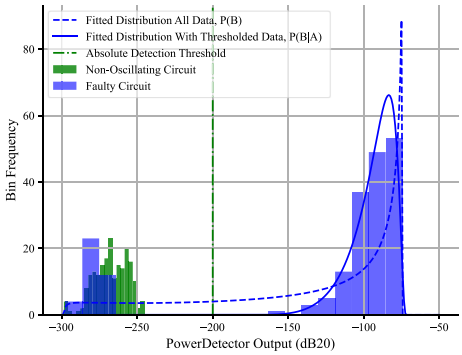


FIGURE 9. Output of strategy 1 test for two faulty circuits (one oscillating in blue, one non-oscillating in green), with P(B) (fitted distribution for all data) and P(B|A) (fitted distribution to thresholded data) fitted.

For each MC run, a zero-voltage, zero-power or zero-frequency result (as discussed in Section III) are considered 100% likely detections of a fault. All other data in the MC run are fitted to an appropriate distribution (Fig. 9) to determine probability of detection given detection thresholds.

As some results are disregarded (due to threshold limiting) in fitting the distribution, a conditional probability condition is applied [59]. *P(B)* is the probability that the random variable (in this case, the measured OBT or OBIST quantity) falls within some prescribed threshold range [x_1, x_2], according to some fitted distribution function as pictured in Fig. 9 and Fig. 10. *P(A)* is the probability of a nonzero detection:

$$P(A) = 1 - \frac{N_Z}{N_T}, \tag{1}$$

where N_Z is the number of zero-detections in the dataset and N_T the total number of simulations.

To calculate the probability of random variable B falling in the range $[x_1, x_2]$, it is necessary to include the probability non-zero detection as well. The addition law of probability gives:

$$P(B \cup A) = P(B) + P(A) - P(B \cap A), \tag{2}$$

which leads to:

$$P(B \cap A) = P(B) + P(A) - P(B \cup A). \tag{3}$$

The conditional probability for any two variables is given by Kolmogorov definition:

$$P(B|A) \cdot P(A) = P(B \cap A). \tag{4}$$

By substituting in (4) into (3),

$$P(B|A) \cdot P(A) = P(B) + P(A) - P(B \cup A). \tag{5}$$

Since the event B is completely in event A:

$$P(A) = P(B \cup A). \tag{6}$$

Therefore,

$$P(B|A) \cdot P(A) = P(B). \tag{7}$$

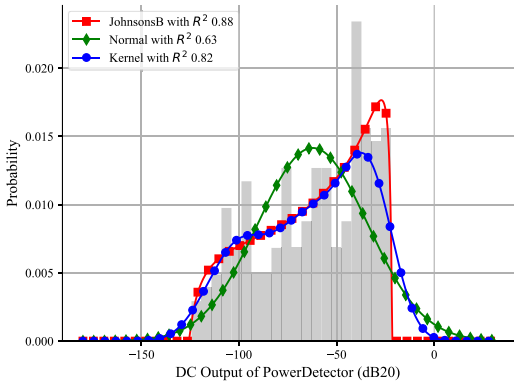


FIGURE 10. Fitted (*B*) distributions to strategy 1 detected data for a faulty case.

The probability that B is between x_1 and x_2 is now given by:

$$P(x_1 < B < x_2) = P(x_1 < B < x_2|A) \cdot P(A). \tag{8}$$

The probability that B is between x_1, x_2 is now calculated as the probability of event B, given event A, is between x_1, x_2 and scaled by the probability of event A. This leads to a more accurate description when all the statistical data is not used to fit the distributions, but still needs to be accounted for.

B. DISTRIBUTION FITTING

Another critical choice in data processing is the choice of distribution to calculate *P(B)*. Several distributions were evaluated (selected based on prior use in Monte Carlo analysis and similarity and visual inspection of sample data), namely the normal Gaussian distribution, the Gaussian distribution with kernel density estimation, and the Johnson S_B bounded distribution. An example dataset, with the three fitted PDFs, is shown in Fig. 10.

A coefficient of determination for each fitted distribution, as a measure of goodness of fit, is calculated as:

$$R^2 = 1 - \frac{SS_{RES}}{SS_{TOT}}, \tag{9}$$

where SS_{TOT} is the total sum of squares and SS_{RES} is the sum of the squares of the residuals.

This fitting and R^2 calculation are then done for all faults, supply voltages and temperatures, an example result of which is shown in Fig. 11.

The mean and standard deviation of the 2D arrays of R^2 were then calculated for each fault and for each strategy, a sample of which is shown in Fig. 12 for strategy 1 (measuring only P_1). The mean and standard deviation of this graph for each fit is then used as a summary and is tabulated in Table 1.

It is evident that the Gaussian fitting is consistently the least accurate approach, as it cannot model the skewness of the data (which is a result of logarithmic voltage and power detection). For strategies 6, 9, 11, 13-15 the kernel distribution is marginally better than the Johnson's S_B distribution.

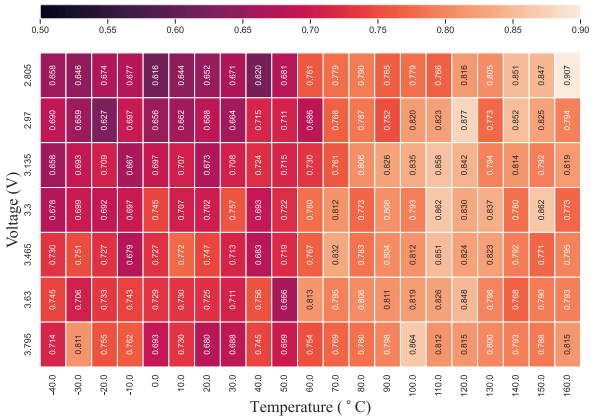


FIGURE 11. R2 array for Gaussian distribution to strategy 1 detected data for a faulty circuit over voltage and temperature variation.

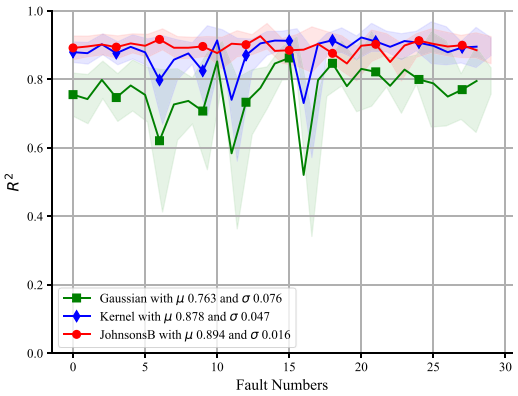


FIGURE 12. R2 for three distribution functions over all faults using strategy 1 detection data, with range shown in shaded colors.

TABLE 1. Summary of R^2 distributions for different PDFs.

	Gaussian		Kernel		Johnson's S_B	
	μ	σ	μ	σ	μ	σ
Strategy 1	0.763	0.076	0.878	0.047	0.894	0.016
Strategy 2	0.764	0.083	0.882	0.058	0.905	0.025
Strategy 3	0.781	0.09	0.897	0.042	0.898	0.018
Strategy 4	0.855	0.032	0.919	0.017	0.903	0.021
Strategy 5	0.815	0.044	0.92	0.017	0.928	0.015
Strategy 6	0.881	0.029	0.953	0.01	0.920	0.019
Strategy 7	0.871	0.029	0.929	0.015	0.914	0.018
Strategy 8	0.822	0.041	0.921	0.017	0.929	0.014
Strategy 9	0.901	0.027	0.962	0.008	0.931	0.016
Strategy 10	0.854	0.032	0.918	0.017	0.902	0.021
Strategy 11	0.867	0.021	0.927	0.006	0.910	0.008
Strategy 12	0.823	0.026	0.922	0.007	0.929	0.007
Strategy 13	0.816	0.031	0.949	0.005	0.872	0.026
Strategy 14	0.849	0.014	0.92	0.007	0.901	0.006
Strategy 15	0.866	0.036	0.929	0.016	0.920	0.024
Average	0.835	0.041	0.922	0.019	0.910	0.017

The Kernel and Johnson's S_B distributions have an R^2 distribution mean of 0.922 and 0.910 respectively, and a variance of 0.019 and 0.017 respectively.

However, the Johnson's S_B variance is more consistently accurate between 0.006 and 0.025 as opposed to the Kernel which varies between 0.005 and 0.058. For this reason, the

Johnson's S_B distribution was chosen as the distribution of choice for all datasets in this study, though its applicability should be interrogated explicitly (using the approach demonstrated here) before applying this analysis to other RFCMOS circuits.

C. FIGURE OF MERIT CALCULATION

In literature on specification-driven testing, probability of test escape $P(T_E)$ and yield loss $P(Y_L)$ are used as a measure for determining the efficacy of a test under investigation [13], [60]. $P(Y_L)$ is defined as functional CUTs that fail the test despite meeting the required performance specification, where $P(T_E)$ is defined as circuits not meeting specification that pass the tests. While the true number of faulty devices that pass testing is a function both of $P(T_E)$ and the probability of a specific fault occurring, this work will focus on the efficacy of the test assuming that a known fault has occurred.

As this work considers structural testing, as opposed to performance testing, performance specifications are not considered in classification. In its absence, a conservative approach is taken, which assumes that any circuit that contains any injected fault, does not meet the specification, irrespective of actual performance. Therefore, a fault-free circuit that fails the threshold detection test is assumed to be part of $P(Y_L)$, and a faulty circuit that passes the test is assumed to be part of $P(T_E)$.

In this paper, each injected catastrophic fault is considered equally probable for the purpose of analysis, and the probability of correctly identifying working and faulty circuits are evaluated as statistically independent processes.

To compare different OBT and OBIST strategies for analogue and RF circuits where the oscillation of the circuit causes a probabilistic random variable (power, voltage or frequency) as an output, an FoM is defined for a specific OBT/OBIST approach where $P(T_E)$ and $P(Y_L)$ are weighted by a differential factor $\delta \in [0,1]$:

$$FoM = \delta \cdot (1 - (PY_L)) + (1 - \delta) \cdot (1 - P(T_E)) \quad (10)$$

The parameter δ in (10) may be used to weigh the FoM in favour of either reduced risk of passing a faulty circuit (leading to lower yield) or lower probability of failing a passing circuit (leading to more test escapes). In the case of $\delta = 0.5$, the penalty of failing a single passing circuit is weighted the same as the penalty of passing a failing circuit, averaged over N possible faults. If the FoM is to be used to optimize test efficacy and minimize cost, it must be informed by the relative cost of test escapes vs. yield loss, as well as a statistical model for injected faults.

In a system where the fault-free CUT is the only one that meets specification, as is assumed here, each CUT and detection threshold selection approach will be associated with a specific $P(Y_L)$. On the other hand, for the i^{th} injected fault, there is a probability that a CUT with that specific fault can escape the test, quantified as T_{Ei}. Since all the faults are simulated using the same number of MC runs, and all the probabilities are scaled using (8), one can calculate the total $P(T_E)$ of the CUT with all possible faults as:

$$P(T_E) = \frac{\sum_i^N P(T_{\mathrm{Ei}})}{N}. \quad (11)$$

Using detection thresholds $x_{1,2}$, as discussed previously, the FoM definition in [28] can be extended on as:

$$FoM = \delta \cdot P(x_1 < X < x_2) + (1 - \delta) \cdot \frac{\sum_i^N 1 - P(x_1 < Y_i < x_2)}{N} \quad (12)$$

where N is the number of possible faults, $P(x_1 < X < x_2) = (1 - P(Y_L))$ is the probability of the nominal circuit's measured output X falling within the thresholds x_1 and x_2 (correct detection of a nonfaulty circuit) and $1 - P(x_1 < Y_i < x_2) = 1 - P(T_{Ei})$ is the probability that the i^{th} faulty circuit's measured output Y_i falls outside of the same thresholds (correct detection of a faulty circuit). Both probabilities are scaled by assuming event A (i.e., that there is some measured quantity due to oscillation) as discussed in Section IV-A. The FoM is further informed by a relative weighting of $P(T_E)$ and $P(Y_L)$, controlled by parameter δ. By setting δ to 0.1, the contribution of $P(Y_L)$ to the FoM is 10% that of the contribution of $P(T_E)$.

From (12) it is evident that the choice of the lower (x_1) and upper (x_2) threshold will have a major impact on the two terms of the FoM calculation. In order to conduct a sensible testing campaign, it should be assumed that the upper and lower thresholds must include, at least to some degree, the working circuit distribution, otherwise the $P(Y_L)$ will be 1 and all the working circuits will be discarded while some non-working circuits might pass the test.

The approach to selecting x_1 and x_2 in this study, is to use a symmetric offset around the mean value of some measurement associated with a working circuit, and to calculate both using the confidence interval (CI) of the distribution $P(X)$. It is shown in Fig. 13 that a smaller choice of δ results in lower impact $P(Y_L)$ on FoM, while a larger δ leads to a higher FoM for wider detection thresholds to reduce the FoM penalty of yield loss. In this work, a δ of 0.1 is used for further analysis, as test escapes are generally considered more expensive than yield loss.

V. THRESHOLD SELECTION APPROACHES

Previous work only considered the CUT, OBT or OBIST circuits under nominal PVT, leading to simple choices for x_1 and x_2 using a nominal distribution $P(X)$. However, as is shown in Fig. 14 and Fig. 15, there is significant variation in X (and, similarly, Y_i) over the temperature for both OBT and OBIST circuits, invalidating the nominal thresholds.

In Fig. 14, the strategy 1 distributions (as discussed in Section III-B) for a nonfaulty CUT are shown for different temperatures, with four thresholding approaches (discussed below) to determine the x_1 and x_2 illustrated as applied at each temperature increment. In Fig. 15, the same four

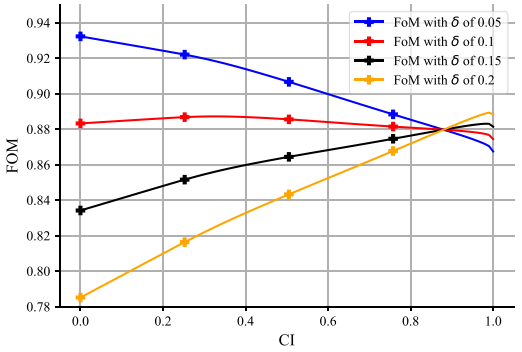


FIGURE 13. FoM vs CI threshold selection approaches for strategy 1 data, for different values of δ.

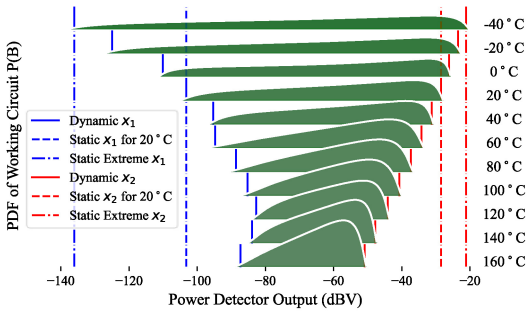


FIGURE 14. *P(B)* for strategy 1 OBIST under temperature variation, on a non-faulty circuit with nominal supply voltage.

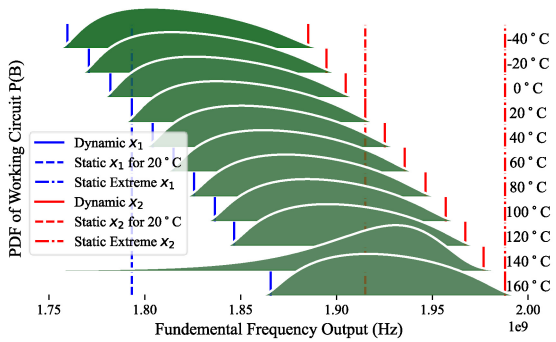


FIGURE 15. *P(B)* for strategy 13 OBT under temperature variation, on a non-faulty circuit with nominal supply voltage.

thresholding approaches are applied for OBT-based detection using strategy 13, for the same incremental temperatures.

It is generally found that $P(X)$ and $P(Y_i)$ are more heavily influenced by ΔT than by ΔV, as changes in the temperature of the circuit lead to far greater changes in the statistical distributions of measured quantities than changes in supply rail voltage. As such, V_{DD}-dependent dynamic thresholding is not investigated here, though the use of bias-aware thresholding (and, in fact, the implementation of bias control in generating more test data [61]) should be considered for future work.

Four approaches to thresholding are investigated systematically (across a V_{DD} range of 2.805-3.795 V and a T range of -40 – 160 °C), as discussed below. These thresholding approaches are different from the strategies discussed in

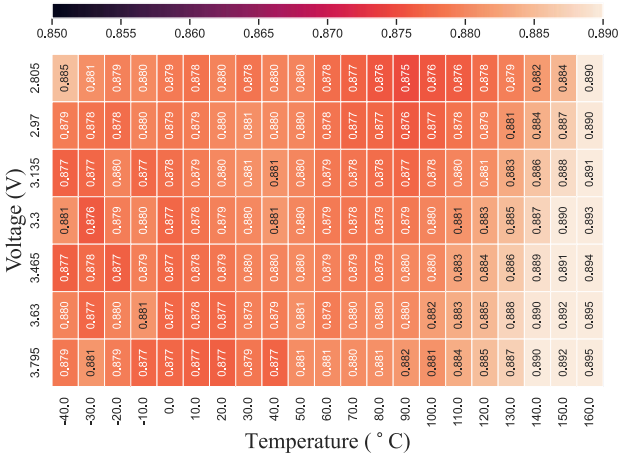


FIGURE 16. FoM heatmap for nominal static threshold approach using strategy 1.

Section III-B, in that they are applied to all 15 strategies and are only used in determining the FoM. Thresholding approach 4 is not visualized in Fig. 14 or Fig. 15, as the noise thresholds are much lower than the pictured outputs.

1) NOMINAL STATIC THRESHOLD APPROACH (APPROACH 1)

The nominal static approach uses the nominal temperature (20 °C) output to determine the threshold values at a CI of 0.9 (coinciding to $\approx 1.64\ \sigma$ for normally distributed data) from the nominal working circuit. With this, a peak FoM of 0.895 is calculated from $P(X)$, (Y_i) and $P(A)$ at 160°C and V_{DD} = 3.795 V. The resulting spread of FoM values in Fig. 16 would indicate reasonable FoM retention above 120°C and across ΔV, due to the narrowing of the distributions with temperature.

2) TEMPERATURE DYNAMIC THRESHOLD APPROACH (APPROACH 2)

The dynamic approach uses an MC simulation at each 10 °C increment of temperature from -40 to 160 °C (maintaining V_{DD} of 3.3V) and re-calculates the thresholds at a CI of 0.9 for the nominal working circuit at each evaluated temperature point. The FoM heatmap generated by this approach, shown in Fig. 17, would indicate high test efficacy across ΔT and ΔV, at the expense of implementation complexity, as accurate thermometers are required on-chip to determine the appropriate threshold values. The result is also subject to low PVT variation in the thermometer circuit itself. As with ADCs, thermometer circuits were not included in this study, to reduce the number of fault simulations and maintain focus on the RF circuit testing.

Due to the δ of 0.1 in the FoM assigning greater weight to $P(T_E)$, and the wider thresholds at lower temperatures of strategy 1, as shown in Fig. 14, the FoM degrades rapidly below 50°C. However, the FoM is greatly improved (compared to nominal static thresholding) between 60°C and 120°C.

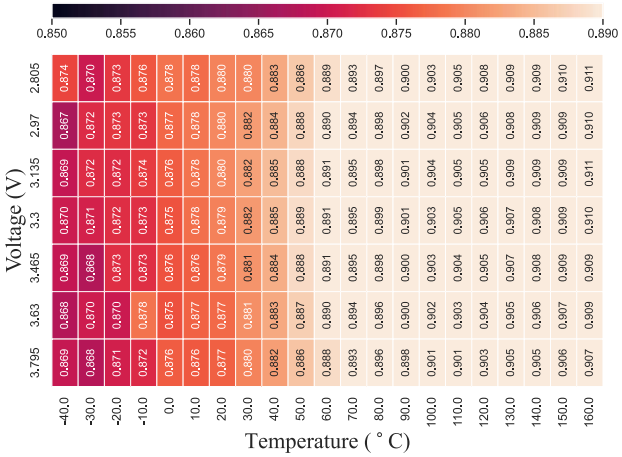


FIGURE 17. FoM heatmap for dynamic threshold approach using strategy 1.

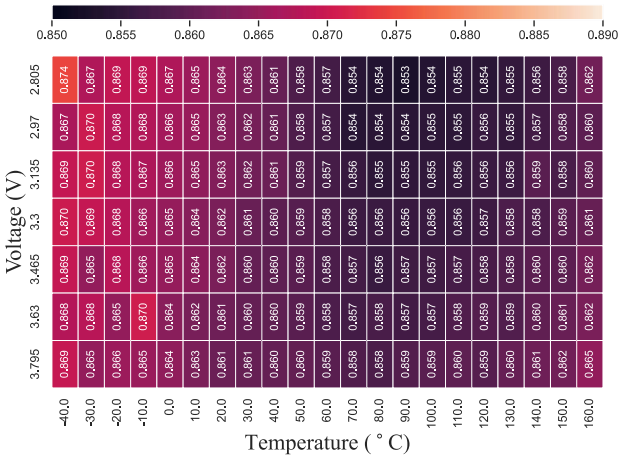


FIGURE 18. FoM heatmap for extreme static threshold approach for strategy 1.

3) EXTREME STATIC THRESHOLD APPROACH (APPROACH 3)

The extreme static approach fixes x_1 and x_2 as the worst-case 0.9 CI values, over all temperature simulations, to ensure that all $P(X)$ distributions fall well within these bounds at higher temperatures (as shown in Fig. 14 and Fig. 15). The resulting FoM heatmap in Fig. 18 would indicate consistent performance across ΔT and ΔV, but consistently lower efficacy than nominal static thresholding and dynamic thresholding. This thresholding technique might be valuable when more weight is assigned to $P(Y_L)$ than to $P(T_E)$

4) NOISE FILTERING THRESHOLD APPROACH (APPROACH 4)

The noise threshold detection approach is the simplest of the four, implementing binary detection of an oscillating tone. It effectively sets x_1 to the same threshold that was used to remove outlier data and x_2 to ∞. The approach assumes that no faulty circuits oscillate; if any P_1 or P_2 value (for OBIST strategies) is detected above the x_1 noise threshold, the circuit is detected as non-faulty. This also applies for the OBT voltage at port 1; if the fundamental tone is detected above the noise threshold, the circuit is detected as nonfaulty. For the frequency in OBT strategies 14 and 15, x_1 is set to 600 MHz, matching the PSS solver lower oscillator limit. This may similarly be expressed as the assumption that $NZ = NT$ in (1), or $P(A) = 0$.

This method yields a similarly consistent FoM across ΔT and ΔV (as shown in Fig. 19), though lower than any of the other approaches. The advantage of this approach is, however, that a simple comparator, rather than a digitizer, an be used for binary fault detection, greatly reducing the complexity of the test circuit.

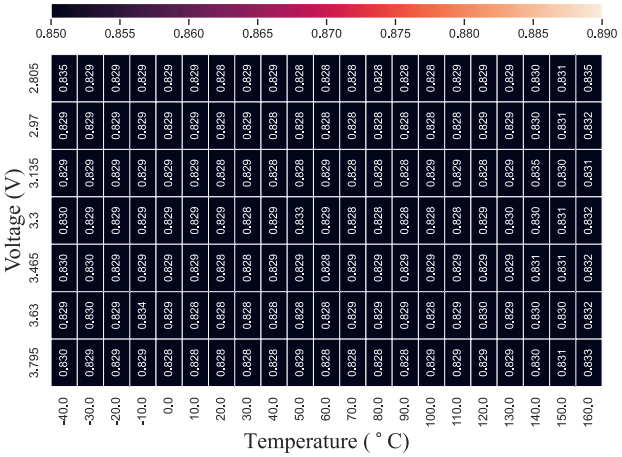


FIGURE 19. FoM heatmap for the noise threshold approach for strategy 1.

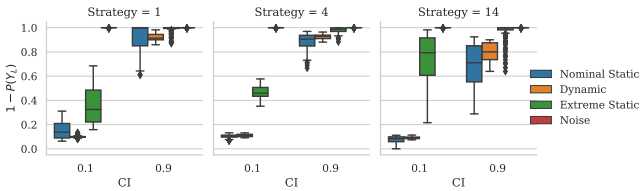


FIGURE 20. 1-$P(Y_L)$ with confidence intervals of 0.1 and 0.9, for all four threshold selection approaches.

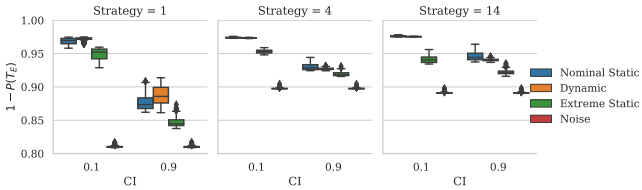


FIGURE 21. 1- $P(T_E)$ with confidence intervals of 0.1 and 0.9, for all four threshold selection approaches.

VI. RESULTS AND DISCUSSION

In this section, the FoM is calculated using (12), across all test strategies, with δ=0.1. However, to gain understanding of the effect of the confidence interval on the FoM, the 1-$P(Y_L)$, 1-$P(T_E)$, and the resulting FoM are shown in Fig. 20-Fig. 22, for test strategies 1, 4, and 14. Note that CI has no effect on noise thresholding.

It is important to note from Fig. 20-Fig. 22 that, when considering $P(Y_L)$ alone, almost no working circuits will be

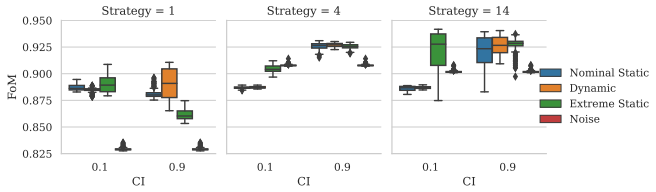


FIGURE 22. The resulting FoM, using (12), with CI's of 0.1 and 0.9, for all four threshold selection approaches.

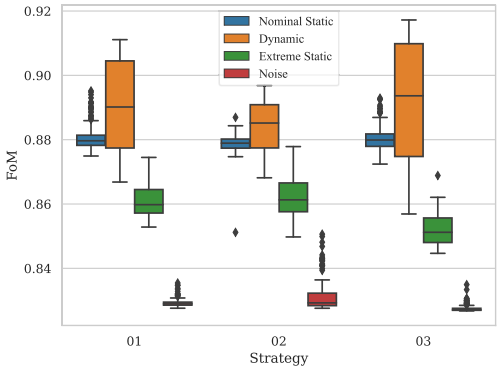


FIGURE 23. FoM comparison for OBIST test strategies 1-3 and all four threshold selection approaches.

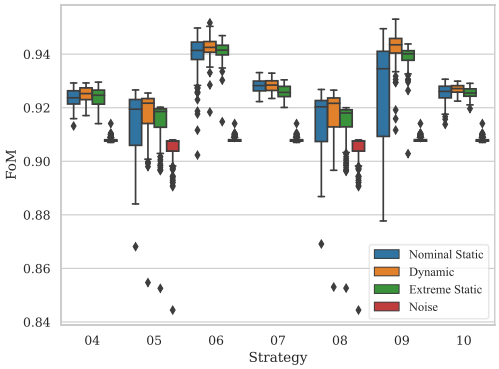


FIGURE 24. FoM comparison for equivalent OBT test strategies 4-10 and all four threshold selection approaches.

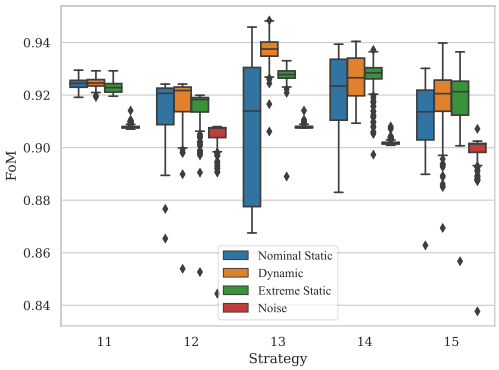


FIGURE 25. FoM comparison for scalar OBT test strategies 11-15 and all four threshold selection approaches.

discarded using the noise threshold approach as 1 - $P(Y_L)$ tends to 1. For a CI value of 0.1 the 1 - $P(Y_L)$ tends to degrade for all the other thresholding approaches, especially the dynamic and nominal static thresholds. Even though the effect of $P(Y_L)$ on the FoM is minimal when $\delta = 0.1$, it still contributes enough to influence the FoM to such a degree that the noise threshold approach will be preferable over all the others in the OBT strategies 4 and 14 (with CI set to 0.1).

Keeping this observation in mind, the data of the heatmaps of Fig. 16-Fig. 19 is now generated for each of the 15 test strategies in Section V, for δ=0.1 and CI = 0.9, and summarized in Fig. 23 for the OBIST approaches (strategies 1-3), Fig. 24 for the power detected OBT approaches (strategies 4-9) and Fig. 25 for the voltage and frequency OBT approaches (strategies 10– 15).

An important initial observation is that the OBT strategies outperformed the OBIST strategies. This may be attributed to the fact that faults in the power detector do not get factored into to the FoM of the OBT, resulting in a higher FoM.

The nominal static threshold, approach 1, has the widest spread in FoM and can be worse than the noise threshold approach, approach 4, at extreme temperatures. This is readily explained by the extreme temperature-dependence on $P(X)$ shown in Fig. 14 and Fig. 15. This threshold approach will, however, perform well if the CUT is operating in a known, temperature stable environment.

When considering OBIST strategies there seems to be very little benefit, in terms of FoM, in enforcing two switching states, with the comparative strategy 3 actually performing worse when extreme static thresholding is applied. While temperature-aware dynamic thresholding outperforms nominal static thresholding in some cases, its benefit varies considerably over test conditions, as evidenced by the wider error boxes.

However, when considering the equivalent power detected OBT strategies, the benefit of switching becomes clearer as the switching strategies (6, 9, 13) outperforms the single state strategies (4, 5, 7, 8, 11 and 12). Strategies 7, 8 and 9, which use a frequency dependent power detector, seems to provide little benefit over the OBT strategies (4, 5 and 6) with no frequency dependence. This would indicate that oscillator power, rather than frequency, is a stronger indicator of faults.

The peak voltage measurement OBT strategies (11, 12 and 13) that measures the voltage at port 1 provide very similar results to that of the equivalent power measurement OBT strategies (4-10) but with less variance, except for the nominal static threshold case with strategy 13. The advantage of total power measurement at RF, as opposed to down conversion or RF digitization, further favours strategies 4-6. The strategies using an off-chip frequency counter (14 and 15) were found to be exhibit the widest variation in FoM values of the OBT strategies.

The results of the best-performing thresholding approach, namely dynamic threshold selection based on temperature, is shown in Table 2 for all the OBT and OBIST strategies,

TABLE 2. Summary of best FoM with the corresponding $P(Y_L)$ and $P(T_E)$ for all strategies for the dynamic threshold selection approach. $\delta = 0.1$.

Strategy	FoM	$P(T_E)$	$P(Y_L)$
1	0.911	$7.85 \cdot 10^{-2}$	$1.82 \cdot 10^{-1}$
2	0.897	$7.7 \cdot 10^{-2}$	$3.39 \cdot 10^{-1}$
3	0.917	$8.81 \cdot 10^{-2}$	$3.5 \cdot 10^{-2}$
4	0.93	$7.12 \cdot 10^{-2}$	$5.72 \cdot 10^{-2}$
5	0.925	$7.7 \cdot 10^{-2}$	$5.2 \cdot 10^{-2}$
6	0.952	$5.26 \cdot 10^{-2}$	$9.41 \cdot 10^{-3}$
7	0.933	$6.59 \cdot 10^{-2}$	$7.79 \cdot 10^{-2}$
8	0.927	$7.44 \cdot 10^{-2}$	$6.46 \cdot 10^{-2}$
9	0.953	$5 \cdot 10^{-2}$	$1.89 \cdot 10^{-2}$
10	0.93	$7.38 \cdot 10^{-2}$	$3.64 \cdot 10^{-2}$
11	0.93	$7.32 \cdot 10^{-2}$	$4.25 \cdot 10^{-2}$
12	0.924	$7.61 \cdot 10^{-2}$	$7.37 \cdot 10^{-2}$
13	0.948	$5.37 \cdot 10^{-2}$	$3.24 \cdot 10^{-2}$
14	0.94	$5.51 \cdot 10^{-2}$	$1 \cdot 10^{-1}$
15	0.94	$5.91 \cdot 10^{-2}$	$7.02 \cdot 10^{-2}$

TABLE 3. Average FoM between threshold approaches for all the strategies.

Strategy	Nominal Static	Dynamic	Extreme Static	Noise	Strategy Means
1	0.881	0.890	0.861	0.829	0.865
2	0.879	0.884	0.862	0.832	0.864
3	0.880	0.892	0.852	0.828	0.863
4	0.926	0.927	0.925	0.908	0.922
5	0.914	0.918	0.915	0.905	0.913
6	0.940	0.942	0.941	0.908	0.933
7	0.928	0.928	0.926	0.908	0.923
8	0.915	0.917	0.915	0.905	0.913
9	0.925	0.942	0.939	0.908	0.929
10	0.925	0.927	0.926	0.908	0.922
11	0.925	0.926	0.926	0.908	0.921
12	0.915	0.917	0.915	0.905	0.913
13	0.907	0.937	0.928	0.908	0.920
14	0.921	0.926	0.927	0.902	0.919
15	0.912	0.917	0.918	0.899	0.912
Approach Means	0.913	0.919	0.912	0.891	0.909

with shaded rows indicating measurements using both states. All fault-free circuits that fail the threshold detection test is assumed to be part of $P(Y_L)$, and all faulty circuits that pass the test is assumed to be part of $P(T_E)$.

Due to this conservative approach, the test escape that correspond to the best FoM (0.953) at $P(T_E) = 5{\cdot}10^{-2}$ is much worse in this study than that of an optimized $P(T_E) = 9.09{\cdot}10^{-4}$ from [16] and $P(T_E) = 1.98{\cdot}10^{-4}$ from [60]. Due to the CI choice of 0.9, the yield loss that correspond to the best FoM in this study is high at $P(Y_L) = 1.89{\cdot}10^{-2}$ compared to that of $P(Y_L) = 9.1{\cdot}10^{-3}$ from [16] and $P(Y_L) = 1.98{\cdot}10^{-4}$ from [60].

$P(T_E)$ may be improved when performance specifications, rather than structural faults, is used in the evaluation, though this may lead to passing of several circuits with structural faults, but that still meet performance specifications. This result may be further refined by augmenting OBT or OBIST measurements with other tests, such as IDDQ measurements [62], [63]. $P(Y_L)$ can be improved by increasing the CI over which the thresholds are selected.

These tabulated results are further evident when considering the fitted distributions of X in green and selected distributions of Y_i in Fig. 26 for T between −20 – 160 °C in 20 °C increments with V = 3.3 V. Strategies 1-3 (with strategy 1 shown in as in Fig. 26 (a)) have wider distributions with, consequently, significant overlap between different Y_i distributions and significantly more overlap between different Y_i distributions and X. This means the faults are not distinguishable from each other, with most faults detected equally well. In strategies 4-15 (shown in Fig. 26 (b)-(e)), however, the nominal distributions are clearly narrower, which illustrates why better fault detection attainable.

Another interesting feature of these results is evident when considering the distributions for some faulty conditions. These include OC on node N0_3, SC between node N0 and N1 and SC between node N2 and N9 to produce the yellow, red and blue distribution respectively. The clear and distinct distribution of the measurements associated with these faults not only improve the FoM, but may also lead to fault diagnosis using secondary OBT testing in future work. Even though the frequency related strategies (14 and 15) results in poor FoM results, they can still be used to isolate and identify specific faults, as shown in Fig. 26 (d) and (e).

A summary of the test results is shown in Table 3, with shaded rows indicating test strategies with two measurement states. The highest overall FoM is for Strategy 6 ($|P_{1OBT} - P_{2OBT}|$, the difference in the total detected power at Port 1 when switching between oscillation states 1 and 2) using nominal static thresholds, though Strategy 6 maintains high FoM across all threshold selection approaches. As this does not necessitate high-speed digitization nor an additional RF test port interface to the chip, its application to this particular CUT would be advantageous.

Considering OBIST approaches with only DC and control interfaces to the chip, Strategy 1 (P_1 (dBV), the power detector DC output for the oscillator in state 1). The approach may be improved with temperature-dependent dynamic threshold selection, but not by a switched oscillation state.

In all cases, frequency information (either in frequency dependent power measurement or oscillation frequency counting) does not add much value to detection efficacy.

VII. CONCLUSION

We have presented an analysis on the efficacy of different OBT and OBIST approaches to feature extraction, and threshold selection, on a 2.4 GHz LNA in 0.35 μm CMOS over process, temperature, and voltage variations. This is the first time that an extensive study has been done on the influence of these choices, and the first that considers the effect of PVT variations on the outputs of OBT or OBIST systems, especially at RF. Furthermore, this study is the first to report on different approaches for threshold selection in the testing circuitry to pass or fail a test when the temperature is varied.

It is shown that OBIST detection provided lower test FoM than off-chip OBT strategies due to the larger quantity of potential faults in the on-chip detection circuitry. It is

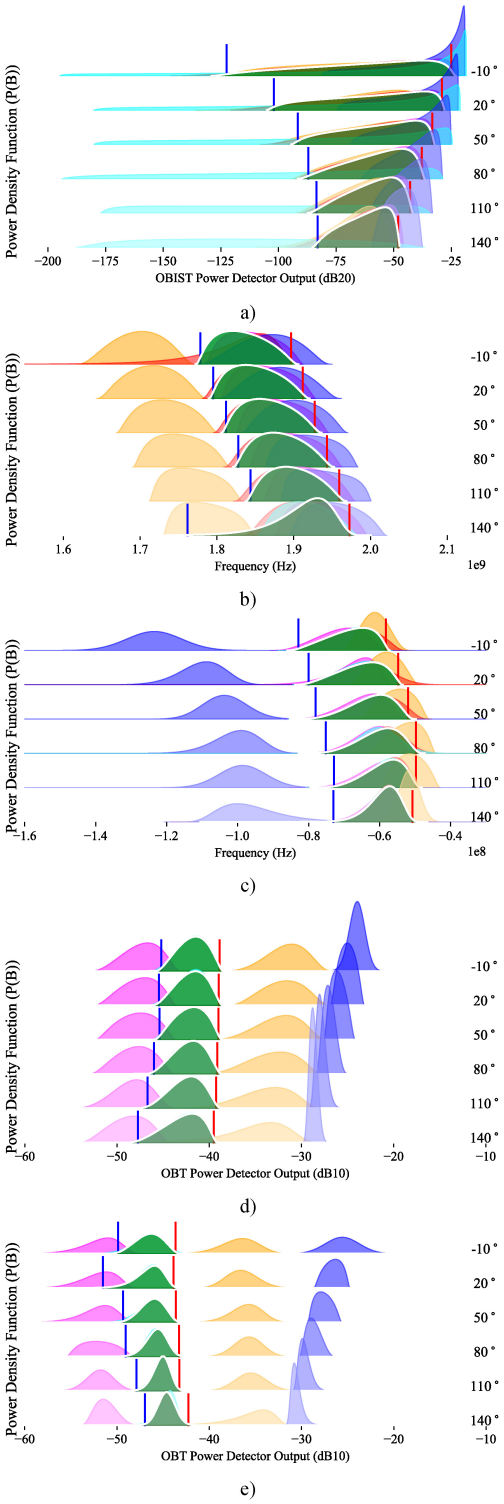


FIGURE 26. Fitted distribution ridge plots for (a) Strategy 1, (b) Strategy 4, (c) Strategy 6, (d) Strategy 14 and (e) Strategy 15, for nominal supply voltage and different temperatures. Nominal working circuit distributions shown in green, with selected faults in blue (SC between N2 and N9), yellow (OC in branch N0_3), red (SC between N0 and N1), cyan (OC in branch N11_3), magenta (SC between N0 and Gnd). Lower x_1 (blue line) and upper x_2 (red line) dynamic thresholds is also shown.

further shown that test FoM is improved at extreme temperatures by selecting dynamic thresholds based on built-in thermometer readings, but that the same dynamic threshold adjustment due to V_{DD} variation is not required. If temperature measurements are not available for the testing, extreme threshold selection is shown to outperform threshold selection for nominal operating data, especially at lower temperatures, as seen in Fig. 16 and Fig. 18. It is, however, found that the FoM is only degraded by an average of 2.303% (compared to extreme threshold selection) if simple noise-thresholded binary detection is used. This latter approach requires neither thermometers, nor digitizers as part of the OBIST circuit, leading to an exceptionally simple BIST design. Finally, it it shown that the value of differential OBT and OBIST detection, as proposed in [40], diminishes over a wide temperature range.

It is anticipated that the analysis approach established here, will be valuable in OBT/OBIST circuit design and threshold selection for a wide variety of designs in future. Future work will include doing a more comprehensive specification test simulation to better evaluate $P(T_E)$ and $P(Y_L)$, also accounting for finite ADC resolution and other non-ideal digitization effects. The study should also be repeated for more advanced nodes, such as 28 nm FDSOI, to see if the principles are maintained in different processes, as well as for parametric circuit faults and performance testing. Finally, the use of bias control as an additional test control [61], multivariate and other statistical test techniques [64] as well as adaptive test thresholding based on known wafer or die data [46], [51] should be considered to improve test discrimination.

REFERENCES

[1] J. Ferrario, R. Wolf, S. Moss, and M. Slamani, "A low-cost test solution for wireless phone RFICs," *IEEE Commun. Mag.*, vol. 41, no. 9, pp. 82–88, Sep. 2003, doi: 10.1109/MCOM.2003.1232241.

[2] J.-F. J. Nowakowski, "An automated LNA/PPA characterization system," in *Proc. 69th ARFTG Conf.*, Jun. 2007, pp. 1–9, doi: 10.1109/ARFTG.2007.5456327.

[3] D. Binu and B. S. Kariyappa, "A survey on fault diagnosis of analog circuits: Taxonomy and state of the art," *AEU Int. J. Electron. Commun.*, vol. 73, pp. 68–83, Mar. 2017, doi: 10.1016/j.aeue.2017.01.002.

[4] M. J. Barragan, H.-G. Stratigopoulos, S. Mir, H. Le-Gall, N. Bhargava, and A. Bal, "Practical simulation flow for evaluating analog/mixed-signal test techniques," *IEEE Design Test*, vol. 33, no. 6, pp. 46–54, Dec. 2016, doi: 10.1109/MDAT.2016.2590985.

[5] L. Abdallah, H.-G. G. Stratigopoulos, S. Mir, and C. Kelma, "RF front-end test using built-in sensors," *IEEE Design Test Comput.*, vol. 28, no. 6, pp. 76–84, Nov./Dec. 2011, doi: 10.1109/MDT.2011.131.

[6] S. R. Das et al., "Testing analog and mixed-signal circuits with built-in hardware—A new approach," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 3, pp. 840–855, Jun. 2007, doi: 10.1109/TIM.2007.894223.

[7] L. S. Milor, "A tutorial introduction to research on analog and mixed-signal circuit testing," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 45, no. 10, pp. 1389–1407, Oct. 1998, doi: 10.1109/82.728852.

[8] C. Chen et al., "Very compact transformer-coupled balun-integrated bandpass filter using integrated passive device technology on glass substrate," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2010, p. 1, doi: 10.1109/MWSYM.2010.5516284.

[9] Y.-R. Wu, Y.-K. Hsieh, P.-C. Ku, and L.-H. Lu, "A built-in gain calibration technique for RF low-noise amplifiers," in *Proc. IEEE 32nd VLSI Test Symp. (VTS)*, Apr. 2014, pp. 1–6, doi: 10.1109/VTS.2014.6818776.

[10] J.-Y. Ryu and B. C. Kim, "Low-cost test technique using a new RF BIST circuit for 4.5–5.5GHz low noise amplifiers," *Microelectron. J.*, vol. 36, no. 8, pp. 770–777, Aug. 2005, doi: 10.1016/j.mejo.2005.01.002.

[11] K. Beznia, A. Bounceur, R. Euler, and S. Mir, "A tool for analog/RF BIST evaluation using statistical models of circuit parameters," *ACM Trans. Des. Autom. Electron. Syst.*, vol. 20, no. 2, pp. 1–22, Mar. 2015, doi: 10.1145/2699837.

[12] L. Abdallah, H.-G. Stratigopoulos, C. Kelma, and S. Mir, "Sensors for built-in alternate RF test," in *Proc. 15th IEEE Eur. Test Symp.*, May 2010, pp. 49–54, doi: 10.1109/ETSYM.2010.5512783.

[13] H.-G. Stratigopoulos, S. Mir, and A. Bounceur, "Evaluation of analog/RF test measurements at the design stage," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 28, no. 4, pp. 582–590, Apr. 2009, doi: 10.1109/TCAD.2009.2016136.

[14] D. Munzer, N. S. Mannem, and H. Wang, "A single-ended coupler-based VSWR resilient joint mm-Wave true power detector and impedance sensor," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 6, pp. 812–815, Jun. 2021, doi: 10.1109/LMWC.2021.3068012.

[15] S. Makhsuci and M. Ehsanian, "Oscillation-based test for measuring 1dB gain compression point of power amplifiers," in *Proc. Iranian Conf. Electr. Eng. (ICEE)*, May 2018, pp. 190–195, doi: 10.1109/ICEE.2018.8472454.

[16] A. Dimakos, H.-G. Stratigopoulos, A. Siligaris, S. Mir, and E. De Foucauld, "Parametric built-in test for 65nm RF LNA using non-intrusive variation-aware sensors," *J. Electron. Test.*, vol. 31, no. 4, pp. 381–394, Aug. 2015, doi: 10.1007/s10836-015-5534-4.

[17] H.-G. Stratigopoulos and Y. Makris, "Error moderation in low-cost machine-learning-based analog/RF testing," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 27, no. 2, pp. 339–351, Feb. 2008, doi: 10.1109/TCAD.2007.907232.

[18] D.-H. Kim, S. Cha, and L. S. Milor, "Built-in self-test for bias temperature instability, hot-carrier injection, and gate oxide breakdown in embedded DRAMs," *Microelectron. Rel.*, vol. 55, nos. 9–10, pp. 2113–2118, Aug. 2015, doi: 10.1016/j.microrel.2015.06.077.

[19] K. Arabi and B. Kaminska, "Testing analog and mixed-signal integrated circuits using oscillation-test method," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 16, no. 7, pp. 745–753, Jul. 1997, doi: 10.1109/43.644035.

[20] K. Arabi and B. Kaminska, "Parametric and catastrophic fault coverage of analog circuits in oscillation-test methodology," in *Proc. 15th IEEE VLSI Test Symp.*, 1997, pp. 166–171, doi: 10.1109/VTEST.1997.600246.

[21] K. Arabi and B. Kaminska, "Oscillation-test methodology for low-cost testing of active analog filters," *IEEE Trans. Instrum. Meas.*, vol. 48, no. 4, pp. 798–806, Aug. 1999, doi: 10.1109/19.779176.

[22] L. Kladovščikov and R. Navickas, "Application of oscillation-based self-testing systems for higher order active RC low-pass filters," in *Proc. 43rd Int. Conf. Telecommun. Signal Process. (TSP)*, Jul. 2020, pp. 369–372, doi: 10.1109/TSP49548.2020.9163431.

[23] M. Margalef-Rovira, M. J. Barragan, E. Sharma, P. Ferrari, E. Pistono, and S. Bourdel, "An oscillation-based test technique for on-chip testing of mm-Wave phase shifters," in *Proc. IEEE 36th VLSI Test Symp. (VTS)*, Apr. 2018, pp. 1–6, doi: 10.1109/VTS.2018.8368622.

[24] M. Petrović and M. Milić, "Analog device design for testability in the case of oscillation based testing," in *Proc. IEEE 30th Int. Conf. Microelectron. (MIEL)*, Oct. 2017, pp. 283–286, doi: 10.1109/MIEL.2017.8190122.

[25] M. Ballot and T. Stander, "A RF amplifier with oscillation-based BIST based on differential power detection," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2021, pp. 1–4, doi: 10.1109/ISCAS51556.2021.9401388.

[26] D. Arbet, V. Stopjaková, L. Majer, G. Gyepes, and G. Nagy, "New OBIST using on-chip compensation of process variations toward increasing fault detectability in analog ICs," *IEEE Trans. Nanotechnol.*, vol. 12, no. 4, pp. 486–497, Jul. 2013, doi: 10.1109/TNANO.2013.2251656.

[27] K. Arabi and B. Kaminska, "Oscillation-test strategy for analog and mixed-signal integrated circuits," in *Proc. 14th VLSI Test Symp.*, 1996, pp. 476–482, doi: 10.1109/VTEST.1996.510896.

[28] T. Stander, P. Petrashin, L. Toledo, W. Lancioni, C. Vazquez, and F. C. Dualibe, "Influence of oscillator topology on fault sensitivity in oscillation based testing (OBT) of OTAs," in *Proc. Argentine Conf. Electron. (CAE)*, Mar. 2019, pp. 1–5, doi: 10.1109/CAE.2019.8709294.

[29] P. A. Petrashin, L. E. Toledo, W. J. Lancioni, C. Vazquez, T. Stander, and F. C. Dualibe, "Influence of passive oscillator component variation on OBT sensitivity in OTAs," in *Proc. IEEE 19th Latin-Amer. Test Symp. (LATS)*, Mar. 2018, pp. 1–4, doi: 10.1109/LATW.2018.8349689.

[30] M.-U. Hasan, Y. Zhu, and Y. Sun, "Oscillation-based DFT for second-order bandpass OTA-C filters," *Circuits Syst. Signal Process.*, vol. 37, no. 5, pp. 1807–1824, May 2017, doi: 10.1007/s00034-017-0648-9.

[31] P. Petrashin, L. Toledo, W. Lancioni, P. Osuch, and T. Stander, "Oscillation-based test applied to a wideband CCII," *VLSI Des.*, vol. 2017, pp. 1–6, May 2017, doi: 10.1155/2017/5075103.

[32] P. A. Petrashin, L. E. Toledo, W. Lancioni, P. J. Osuch, and T. Stander, "Oscillation-based test in a CCII-based bandpass filter," in *Proc. IEEE 8th Latin Amer. Symp. Circuits Syst. (LASCAS)*, Feb. 2017, pp. 1–4, doi: 10.1109/LASCAS.2017.7948042.

[33] K. Suenaga, E. Isern, R. Picos, S. Bota, M. Roca, and E. García-Moreno, "Application of predictive oscillation-based test to a CMOS OpAmp," *IEEE Trans. Instrum. Meas.*, vol. 59, no. 8, pp. 2076–2082, Aug. 2010, doi: 10.1109/TIM.2009.2031381.

[34] G. Peretti, E. Romero, and C. Marqués, "On the ability of oscillation-based test for detecting deviation faults in switched-capacitor ladder filters," *Electr. Eng.*, vol. 90, no. 2, pp. 127–141, Nov. 2007, doi: 10.1007/s00202-007-0065-3.

[35] E. Romero, G. Peretti, G. Huertas, and D. Vázquez, "Test of switched-capacitor ladder filters using OBT," *Microelectron. J.*, vol. 36, no. 12, pp. 1073–1079, Dec. 2005, doi: 10.1016/j.mejo.2005.04.061.

[36] G. Peretti, E. Romero, and C. Marqués, "Testing digital low-pass filters using oscillation-based test," *Microprocess. Microsyst.*, vol. 32, no. 1, pp. 1–9, Feb. 2008, doi: 10.1016/j.micpro.2007.01.005.

[37] S. Callegari, "Introducing complex oscillation based test: An application example targeting analog to digital converters," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2008, pp. 320–323, doi: 10.1109/ISCAS.2008.4541419.

[38] J. J. P. Venter and T. Stander, "Single-ended oscillation-based test technique for passive RF phase shifters," in *Proc. 15th Int. Conf. Adv. Technol. Syst. Serv. Telecommun. (TELSIKS)*, Oct. 2021, pp. 103–106, doi: 10.1109/TELSIKS52058.2021.9606315.

[39] A. Goyal, M. Swaminathan, A. Chatterjee, D. Howard, and J. D. Cressler, "A self-testable SiGe LNA and built-in-self-test methodology for multiple performance specifications of RF amplifiers," in *Proc. 13th Int. Symp. Qual. Electron. Des. (ISQED)*, Mar. 2012, pp. 7–12, doi: 10.1109/ISQED.2012.6187467.

[40] H. P. Nel, T. Stander, and F. C. Dualibe, "Built-in oscillation-based self-testing of a 2.4 GHz LNA in 0.35μm CMOS," in *Proc. 25th IEEE Int. Conf. Electron. Circuits Syst. (ICECS)*, Dec. 2018, pp. 837–840, doi: 10.1109/ICECS.2018.8618052.

[41] K. Jayaraman, Q. Khan, B. Chi, W. Beattie, Z. Wang, and P. Chiang, "A self-healing 2.4GHz LNA with on-chip S11/S21 measurement/calibration for in-situ PVT compensation," in *Dig. Papers IEEE Radio Freq. Integr. Circuits Symp.*, 2010, pp. 311–314, doi: 10.1109/RFIC.2010.5477307.

[42] G. Zhang and R. Farrell, "An embedded rectifier-based Built-in-Test circuit for CMOS RF circuits," in *Proc. IEEE Int. Conf. Electron. Circuits Syst.*, 2006, pp. 612–615, doi: 10.1109/ICECS.2006.379863.

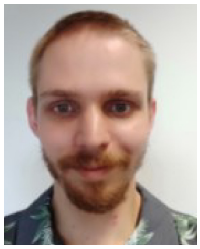
[43] D. C. Howard, T. D. England, N. E. Lourenco, A. S. Cardoso, and J. D. Cressler, "An on-chip SiGe HBT characterization circuit for use in self-healing RF systems," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting (BCTM)*, Sep. 2013, pp. 203–206, doi: 10.1109/BCTM.2013.6798176.

[44] E. Cohen, A. Israel, O. Degani, and D. Ritter, "High sensitivity detector with robust PVT performance for 60GHz BiST phased array systems in 90nm CMOS," in *IEEE 12th Topical Meeting Silicon Monolith. Integr. Circuits RF Syst. (SiRF) Dig. Papers*, 2012, pp. 211–214, doi: 10.1109/SiRF.2012.6160149.

[45] A. Goyal, M. Swaminathan, A. Chatterjee, D. C. Howard, and J. D. Cressler, "A new self-healing methodology for RF amplifier circuits based on oscillation principles," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 20, no. 10, pp. 1835–1848, Oct. 2012, doi: 10.1109/TVLSI.2011.2163953.

[46] H. G. Stratigopoulos and C. Streitwieser, "Adaptive test with test escape estimation for mixed-signal ICs," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 37, no. 10, pp. 2125–2138, Oct. 2018, doi: 10.1109/TCAD.2017.2783302.

[47] E. Yilmaz, S. Ozev, and K. M. Butler, "Adaptive quality binning for analog circuits," in *Proc. 18th IEEE Eur. Test Symp. (ETS)*, May 2013, pp. 1–6, doi: 10.1109/ETS.2013.6569357.
[48] E. Yilmaz, S. Ozev, and K. M. Butler, "Per-device adaptive test for analog/RF circuits using entropy-based process monitoring," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 21, no. 6, pp. 1116–1128, Jun. 2013, doi: 10.1109/TVLSI.2012.2205027.
[49] H.-G. Stratigopoulos and S. Mir, "Adaptive alternate analog test," *IEEE Design Test Comput.*, vol. 29, no. 4, pp. 71–79, Aug. 2012, doi: 10.1109/MDT.2012.2205480.
[50] I. Polian, B. Becker, S. Hellebrand, H.-J. Wunderlich, and P. Maxwell, "Towards variation-aware test methods," in *Proc. 16th IEEE Eur. Test Symp. (ETS)*, 2011, pp. 219–225, doi: 10.1109/ETS.2011.51.
[51] E. Yilmaz, S. Ozev, and K. M. Butler, "Adaptive test flow for mixed-signal/RF circuits using learned information from device under test," in *Proc. IEEE Int. Test Conf.*, Nov. 2010, pp. 1–10, doi: 10.1109/TEST.2010.5699271.
[52] E. Yilmaz, S. Ozev, O. Sinanoglu, and P. Maxwell, "Adaptive testing: Conquering process variations," in *Proc. 17th IEEE Eur. Test Symp. (ETS)*, 2012, pp. 1–6, doi: 10.1109/ETS.2012.6233045.
[53] D. De Jonghe, E. Maricau, G. Gielen, T. McConaghy, B. Tasić, and H. Stratigopoulos, "Advances in variation-aware modeling, verification, and testing of analog ICs," in *Proc. Des. Autom. Test Europe Conf. Exhibit. (DATE)*, 2012, pp. 1615–1620, doi: 10.1109/date.2012.6176730.
[54] C. Zhai, H.-Y. Liu, and K.-K. M. Cheng, "Single-chip CMOS reconfigurable dual-band tri-mode high-efficiency RF amplifier design," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 3, pp. 868–872, Mar. 2021, doi: 10.1109/TCSII.2020.3022908.
[55] J. Altet et al., "BPF-based thermal sensor circuit for on-chip testing of RF circuits," *Sensors*, vol. 21, no. 3, p. 805, Jan. 2021, doi: 10.3390/s21030805.
[56] S. Nejadhasan, F. Zaheri, E. Abiri, and M. R. Salehi, "PVT-compensated low-voltage and low-power CMOS LNA for IoT applications," *Int. J. RF Microw. Comput. Eng.*, vol. 30, no. 11, pp. 1–16, Nov. 2020, doi: 10.1002/mmce.22419.
[57] T. Kim, D. Im, and K. Kwon, "360-μW 4.1-dB NF CMOS MedRadio receiver RF front-end with current-reuse Q-boosted resistive feedback LNA for biomedical IoT applications," *Int. J. Circuit Theory Appl.*, vol. 48, no. 4, pp. 502–511, Apr. 2020, doi: 10.1002/cta.2772.
[58] H. G. Stratigopoulos, S. Mir, E. Acar, and S. Ozev, "Defect filter for alternate RF test," in *Proc. 15th IEEE Eur. Test Symp. (ETS)*, 2010, pp. 265–270, doi: 10.1109/ETSYM.2010.5512726.
[59] A. Davies, "Book review: Applied statistics and probability for engineers: D. C. MONTGOMERY and G. C. RUNGER," *Int. J. Electr. Eng. Educ.*, vol. 32, no. 3, pp. 281–282, Jul. 1995, doi: 10.1177/002072099503200317.
[60] K. Beznia, A. Bounceur, S. Mir, and R. Euler, "Statistical modelling of analog circuits for test metrics computation," in *Proc. 8th Int. Conf. Des. Technol. Integr. Syst. Nanoscale Era (DTIS)*, Mar. 2013, pp. 25–29, doi: 10.1109/DTIS.2013.6527772.
[61] A. Zjajo and J. P. de Gyvez, "Evaluation of signature-based testing of RF/analog circuits," in *Proc. Eur. Test Symp. (ETS)*, 2005, pp. 62–67, doi: 10.1109/ETS.2005.22.
[62] J. P. Hurst and A. D. Singh, "A differential built-in current sensor design for high-speed IDDQ testing," *IEEE J. Solid-State Circuits*, vol. 32, no. 1, pp. 122–125, Jan. 1997, doi: 10.1109/4.553192.
[63] M. Sidiropulos, V. Stopjakova, and H. Manhaeve, "Implementation of a BIC monitor in a new analog BIST structure," in *Dig. Papers IEEE Int. Workshop IDDQ Test.*, 1996, pp. 59–63, doi: 10.1109/IDDQ.1996.557817.
[64] K. Huang, H.-G. Stratigopoulos, L. Abdallah, S. Mir, and A. Bounceur, "Multivariate statistical techniques for analog parametric test metrics estimation," in *Proc. 8th Int. Conf. Des. Technol. Integr. Syst. Nanoscale Era (DTIS)*, 2013, pp. 6–11, doi: 10.1109/DTIS.2013.6527768.



HENDRIK P. NEL received the first B.Eng. degree in electronic engineering and the second B.Eng. degree (Hons.) in microelectronic engineering from the University of Pretoria, Pretoria, South Africa, in 2017 and 2019, respectively, where he is currently pursuing the master's degree in microelectronic engineering.

Since January 2021, he has been serving as an RF/MMIC Engineer with Multifractal Semiconductors (Pty) Ltd., Pretoria. His current research interests include oscillation-based testing of integrated microwave active devices in CMOS.

FORTUNATO CARLOS DUALIBE (Senior Member, IEEE) received the electrical–electronic engineering degree from the Universidad Nacional de Córdoba, Argentina, in 1986, and the Licentiate and Ph.D. degrees in applied sciences from the Université Catholique de Louvain, Belgium, in 1994 and 2001, respectively.

From 1987 to 1990, he was a Technical Supervisor of INTERCORD Video-Games. From 1990 to 1994, he was a Research Fellow with the Research Agency of Córdorba(CONICOR). From 1995 to 2006, he was a Full Professor with the Facultad de Ingeniería, Universidad Católica de Córdorba, Argentina. From 2007 to 2009, he joined FREESCALE Semiconductors as a Senior Analog Designer. At the end of 2009, he participated as an Invited Lecturer in the training program IC-Brasil sponsored by CADENCE. Since December 2009, he has been an Associate Professor with the Université de Mons, Belgium, where he leads the Analog Design Group of the Electronics and Microelectronics Department. His research interests include the design and test of analog and mixed-signal integrated circuits, low-power low-voltage microelectronics, power management, and energy harvesting circuits.

TINUS STANDER (Senior Member, IEEE) received the B.Eng. and Ph.D. degrees in electronic engineering from the University of Stellenbosch, Stellenbosch, South Africa, in 2005 and 2009, respectively.

From 2010 to 2012, he was an RF and Microwave Engineer with Denel Dynamics (a division of Denel SOC Ltd.), Irene, South Africa. In 2013, he joined the Department of Electrical, Electronic and Computer Engineering, Carl and Emily Fuchs Institute for Microelectronics, University of Pretoria, Pretoria, South Africa, where he currently serves as an Associate Professor and the Principal Investigator of Microwave and mm-Wave Microelectronics, with personal research interest in the application of distributed passives on-chip and built-in self-testing. He serves as a Scientific Advisor to Multifractal Semiconductors (Pty.) Ltd., Pretoria. He is also registered as a Professional Engineer with the Engineering Council of South Africa.