Latency Characterization and Performance Evaluation of Synchronized Daisy-Chain EtherCAT Networks Using Standard Cable Pairs and Open-Source Master Solutions

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***Abstract*—EtherCAT is a real-time industrial variant of Ethernet that enables dynamic, time-sensitive data transmission. Most wired Ethernet setups use standard Ethernet cables and the Media Independent Interface (MII) for Layer two connectivity. This work reflects real-world setups that predominantly rely on standard Ethernet pairs cabling and MII connections. The contribution encompasses an empirical evaluation of the performance aspects, exhibited by the EtherCAT network structured upon standard cable pairs technology. This comprehensive assessment is executed through a rigorously designed experimental campaign, specifically tailored for latency measurement purposes. Furthermore, to fortify the analytical approach, the study integrates the methodology of experimental design, a packet analysis tool, and an open-source master controller. A standards-compliant EtherCAT configuration, and a comprehensive experimental campaign was conducted to evaluate network performance, with particular emphasis on latency and robustness under synchronized communication conditions. The results reveal deterministic inter-packet gap measurements of 0.5 ms at the packet layer, a delay of 1.5 ms observed at the frame layer, and physical-layer latency measured at 1.5 µs, under a moderate network load. To ensure rigor and reproducibility, this study combines packet-level trace analysis, open-source EtherCAT masters, and a cost-effective, hardware-independent test setup. A Design of Experiments (DoE) approach was used to assess synchronization performance and identify key parameters.**

***Index Terms*—EtherCAT, Packet Analyzer, Design of Experiment, Synchronization, IgH master, ANOVA, Industrial Automation, Distributed Clock**

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I. Introduction

A. Background

IN In recent years, fieldbus network technologies have been widely adopted in the realm of industrial automation, serving as a viable alternative to the conventional practice of hardwiring input/output connections for programmable automata. These technologies have facilitated the emergence of expansive command and control systems. Nevertheless, as Central Processing Unit (CPU) capabilities, especially in the domain of industrial computers, continue to advance, fieldbuses have come to represent significant bottlenecks, ultimately constraining the performance of automated systems. Given that control architectures often consist of a cyclically structured hierarchy of diverse hardware and software subsystems, response times can extend to three to five times the duration required for practical automata processing.

In the context of interconnecting multiple automated systems, Ethernet presents itself as an intriguing choice. A communication bus must satisfy

Table I: Comparison of Existing EtherCAT Latency Studies Based on Key Criteria

Study	DoE Methodology	Open Source Master	MII Connection	PHY layer delays
Sung et al. (2013) [1]	x	x	x	Not specified
Wang et al. (2014) [2]	x	x	x	Not measured
Corrêa and Almeida (2019) [3]	x	x	✓	0.335 µs
Zhang et al. (2024) [4]	x	✓	x	Not explicitly stated
Lee and Park (2022) [5]	✓	x	✓	1.2 µs
This Work	✓	✓	✓	1.5 µs

certain key criteria, including real-time capabilities and the capacity to handle small-sized data packets, all while maintaining cost-effectiveness.

Numerous proposals have been put forth to enhance the real-time capabilities of Ethernet networks. Some solutions are grounded in protocol adaptations that incorporate support for Carrier-Sense Multiple Access with Collision Detection (CSMA/CD) (responsible for the non-deterministic behavior inherent in the IEEE 802.3 standard) and the implementation of additional mechanisms designed to govern data circulation within the network within predetermined time intervals [6], [7].

Alternatively, other solutions advocate for the integration of switches, a strategy that allows for the segmentation of collision-free domain networks, thereby facilitating the controlled and precise distribution of data packets over time. These approaches prove effective in terms of data transfer and the systematic redirection of data to controllers. However, it is important to note that the latency associated with input readings is often heavily contingent on the specific implementation chosen [8] and [9], [10], [11]. Each piece of equipment employs Ethernet frames individually, resulting in a fundamentally low effective data rate. The briefest Ethernet frames consist of 84 bytes, inclusive of the inter-frame delay. [12].

Ethernet for Control Automation Technology (EtherCAT) offers solutions to address these constraints. EtherCAT is the appellation for an Ethernet-based fieldbus technology, endorsed by the EtherCAT Technology Group (ETG), an international consortium comprising more than 140 entities encompassing companies, users, and manufacturers. Notably, EtherCAT is recognized as an International Electrotechnical Commission (IEC) standard.

Under this technology paradigm, Ethernet packets are no longer subjected to reception, interpretation, and storage at each individual device. Instead, EtherCAT slaves engage in data read and write operations during the frame transfer process within the node. Moreover, these slaves exclusively access data packets explicitly designated for their reception. Consequently, the frames experience only a negligible delay of a few nanoseconds.

The utilization of EtherCAT in the context of 5G and emerging 6G networks holds substantial promise and relevance. These next-generation networks demand not only high-speed data transmission but also seamless integration of various devices and systems with ultra-low latency requirements. EtherCAT's inherent real-time capabilities, efficient utilization of Ethernet communication, and deterministic performance make it a compelling choice for supporting critical applications in such advanced network environments. With the proliferation of smart factories, autonomous systems, and Internet of Things (IoT) devices within the 5G and 6G ecosystems, EtherCAT's ability to deliver rapid, synchronized data exchange across a diverse range of interconnected devices can significantly enhance network efficiency, reliability, and overall performance. Furthermore, the EtherCAT ecosystem has a well-established track record in industrial automation, which can serve as a valuable foundation for implementing robust and reliable communication solutions in the rapidly evolving landscape of 5G and 6G networks [13]–[15]. The Ethernet protocol, as stipulated in the IEEE 802.3 standard, retains its integrity without necessitating the implementation of sub-buses at the level of individual terminals. To align with the requirements of electronic terminal equipment, modifications are solely required at the coupler level, specifically pertaining to the physical layer.

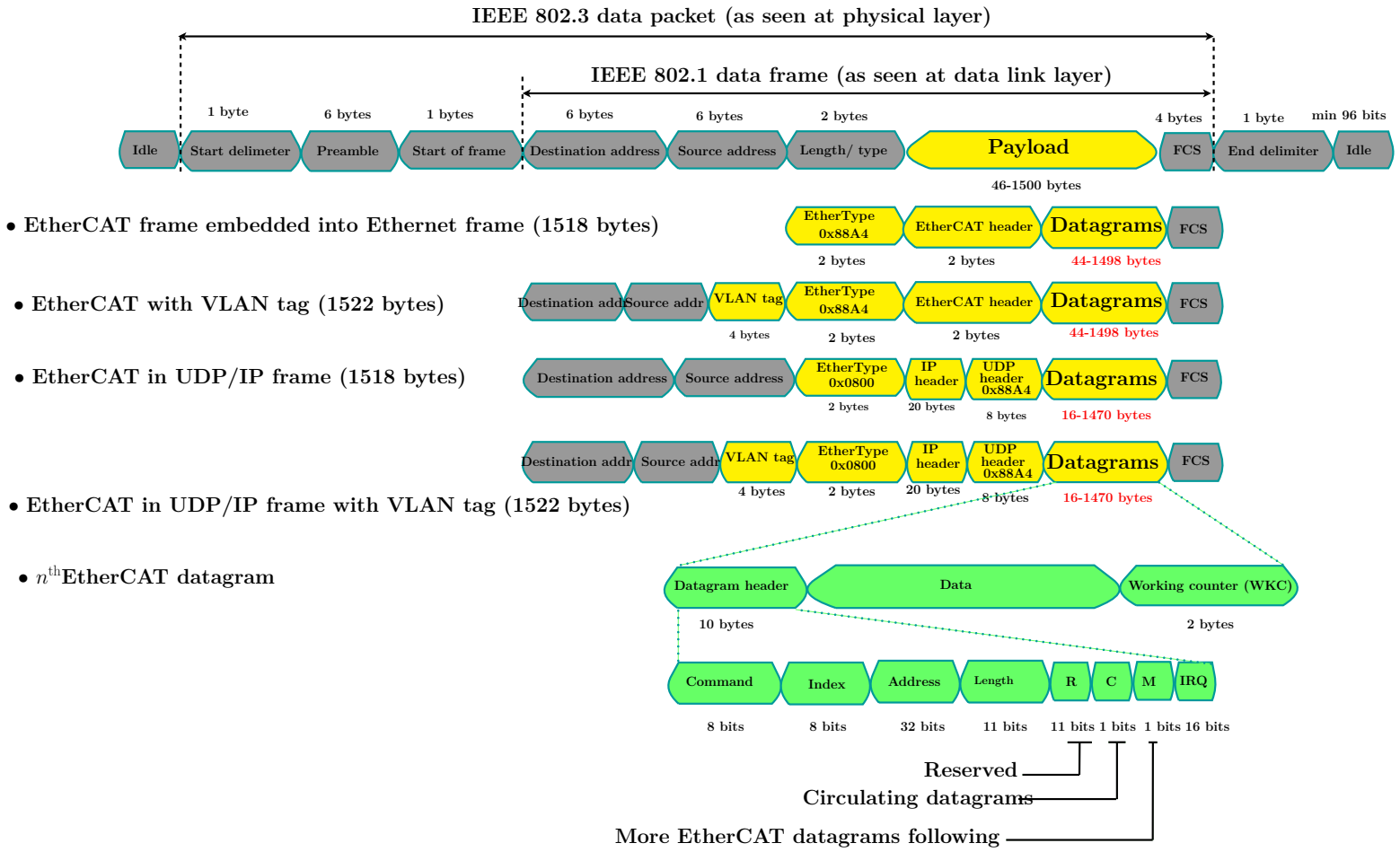


Figure 1: Layered representation of an EtherCAT frame embedded inside a conventional Ethernet frame structure.

B. Related work

Several studies have investigated latency in EtherCAT networks, yet key aspects remain underexplored. For instance, Sung et al. [1] and Wang et al. [2] examined general delay characteristics without considering low-level hardware interfaces or experimental design methodologies. Corrêa and Almeida [3] analyzed ring-based networks and reported PHY-level delays but did not utilize open-source tools or structured parameter evaluation. Zhang et al. [4] explored latency using an open-source master but lacked hardware-specific insights such as MII-based performance. More recently, Lee and Park [5] incorporated DoE to assess timing performance, though without integration of open-source platforms or deep PHY-layer latency validation.

None of these works comprehensively evaluate latency using *Design of Experiments (DoE)* in a *Media Independent Interface (MII)* setting with an *open-source EtherCAT master*. Our study addresses this gap by combining these elements in a reproducible testbed, offering a structured analysis of parameter influence on synchronization. Moreover, it reports quantified delays down to the physical layer, providing insights critical for real-time industrial deployments. Tab. I summarizes key aspects of relevant research, highlighting the gaps current study aims to fill.

C. Contribution of this work

While EtherCAT has been extensively studied in the context of real-time industrial communication, most existing research centers around configurations involving proprietary masters, E-Bus physical layers, or fiber-optic infrastructures. In contrast, this work focuses on a more accessible and practical deployment scenario-an EtherCAT

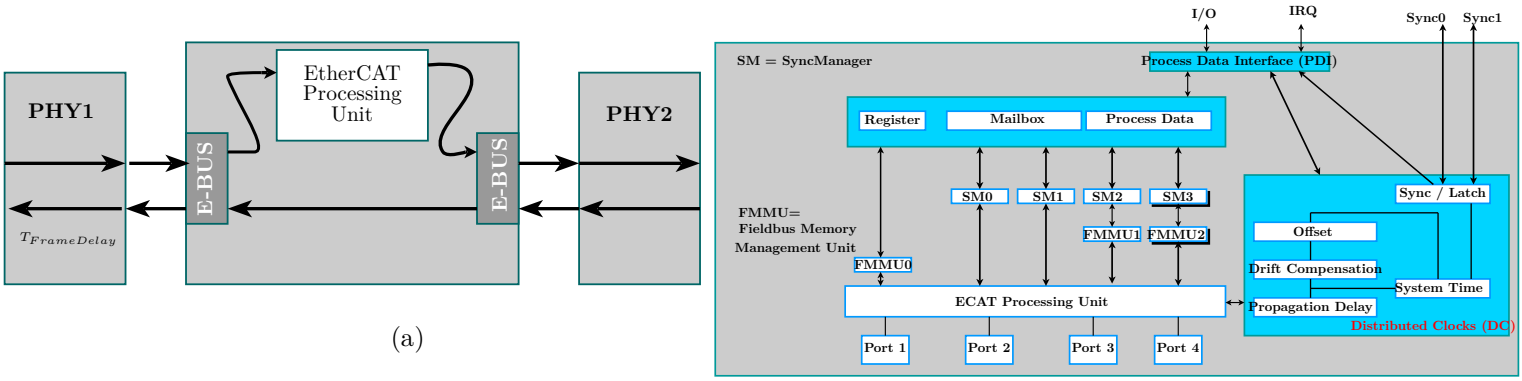


Figure 2: (a) EtherCAT Slave Controller: Block diagram of a typical EtherCAT Slave Controller (ESC) architecture, (b) EtherCAT slave controller structure: Detailed architecture of the EtherCAT Slave Controller, showing core internal modules and data handling pathways.

$$T_{\text{FrameDelay}} = \underbrace{n \times t_{\text{EBUS}}}_{0\,\mu s} + m \times \underbrace{t_{\text{MII}}}_{1.2\,\mu s} + 2 \times \underbrace{t_{\text{cable}}}_{5\,\text{ns/m}} + \underbrace{t_{\text{PD}}}_{1\,\mu s/10\,\text{bytes}} + \underbrace{t_{\text{overhead}}}_{1\,\mu s/10\,\text{bytes}} \quad (1)$$

$$\begin{aligned} n \times t_{\text{EBUS}} &= \text{delay for n slaves with 2 EBUS} \\ m \times t_{\text{MII}} &= \text{delay for m slaves with 2 MII} \\ 2 \times t_{\text{cable}} &= \text{delay for } 100BASE-TX \text{ CAT5 cable } (5\,\text{ns/m}) \\ t_{\text{PD}} &= \text{payload processing delay} \\ t_{\text{overhead}} &= \text{header processing delay} \end{aligned}$$

network utilizing Media Independent Interface (MII) connections over standard Ethernet cabling, integrated with an open-source master controller. This setup closely mirrors real-world conditions in cost-sensitive or open-source industrial environments. To the best of our knowledge, this specific configuration has not been rigorously evaluated in the literature. Furthermore, we adopt a Design of Experiments (DoE) approach to analyze how various configuration parameters-such as Cycle Task (CT) scheduling and Distributed Clock (DC) modes-impact synchronization performance. By combining empirical latency characterization with a reproducible and low-cost evaluation framework, our study aims to bridge the gap between theoretical EtherCAT performance and its practical deployment under MII-based constraints.

The motivation to conduct research on EtherCAT in the context of MII connection is driven by several important factors:

1) Understanding Network Performance: EtherCAT is known for its exceptional real-time capabilities, but its performance can vary based on different network configurations and interfaces. We are motivated to explore how EtherCAT performs when integrated with the MII connection, which is commonly used in Ethernet-based industrial networks. Understanding the performance characteristics, such as latency, bandwidth, and reliability, in this specific context is crucial for optimizing network designs.
2) Industrial Application Relevance: Many industrial systems rely on Ethernet-based communication, and the MII connection is a standard interface for Ethernet. Investigating EtherCAT's performance with MII is directly relevant to industrial automation and control systems, where real-time communication and synchronization are critical. Researchers aim to provide insights and solutions that can enhance the efficiency and reliability of

EtherCAT in industrial applications.

3) Optimizing Latency: Low latency is a key requirement in real-time industrial applications. Researchers are interested in assessing and potentially reducing latency when EtherCAT is used in conjunction with the MII connection. Reducing latency can lead to more responsive and efficient control systems, which is crucial in applications like robotics, machine automation, and process control.
4) Enhancing Network Reliability: Industrial environments can be harsh, and network reliability is paramount. By studying EtherCAT over MII, we can identify potential challenges and vulnerabilities in the network and develop strategies to enhance reliability and fault tolerance. This research contributes to the robustness of EtherCAT-based systems in industrial settings.
5) Practical Implementation: Research on EtherCAT and MII connection provides practical insights into how industries can implement this technology effectively. Researchers aim to provide guidelines, best practices, and
6) Recommendations for configuring and optimizing EtherCAT networks with MII interfaces, making it easier for industrial practitioners to adopt and utilize this technology.

This study presents an empirical examination of a daisy-chain EtherCAT network employing a Linux-based EtherCAT master. From an empirical perspective, this represents the primary novel contribution of this research.

While the EtherCAT-based network has been extensively explored in existing literature, as evidenced by references to prior works [16]–[19], Section II will provide an overview of this technology.

Remarkably, no prior contributions, to the best of our knowledge, have addressed the real-time extrapolation of delays associated with eight EtherCAT Slave Controllers (ESC) equipped with RJ45 connectors. This analysis is conducted through the utilization of both a packet analyzer operating at the data-link layer of the Open Systems Interconnection (OSI) model and real-time measurements facilitated by an oscilloscope and shell scripting. Comprehensive details regarding the experimental setup are elucidated in Section III.

In Section IV, the raw measurement data undergoes rigorous statistical analysis in pursuit of identifying a suitable mathematical model that best fits the observed measurements.

Section V encompasses an exhaustive analysis carried out through the application of the Design of Experiment (DoE) methodology, aiming to present a comprehensive and precise model for delays incurred when deploying the EtherCAT protocol.

Ultimately, the study concludes in Section VI, summarizing the findings and insights drawn from the research endeavor.

II. EtherCAT Overview

The EtherCAT protocol is encapsulated within Ethernet frames via a dedicated 2-byte length field known as “Ethertype,” as depicted in Fig. 1. This encapsulation includes a sequence of subtelegrams that target specific memory areas within the image logic process, with the potential to encompass sizes as large as 4 gigabytes (GB). Significantly, the order in which EtherCAT Slave Controllers (ESCs) are physically connected does not dictate the data sequence, allowing for flexible addressing in any order. Direct Ethernet frame transfer is employed when there is a demand for high performance, particularly in scenarios where EtherCAT components operate within a single subnet.

EtherCAT’s applicability extends beyond single subnets. The EtherCAT User Datagram Protocol (UDP) facilitates the encapsulation of the EtherCAT protocol within Internet Protocol (IP) datagrams, enabling communication across multiple subnets via routers. In such configurations, performance relies on the real-time network’s capabilities and the specific Ethernet implementation. Notably, standard Ethernet patch cables offer the option of transmitting signals in either Ethernet (100Base-TX) or E-bus mode. The Fast Ethernet architecture accommodates cable lengths of up to 100 m between two network elements, while the E-bus design is optimized for distances of up to 10 meters. Furthermore, in terms of network expansion, the capability to connect up to 65535 elements is attainable [20].

The current operational framework is predicated upon the encapsulation of an EtherCAT frame

within an Ethernet frame, the latter having a standard size of 1518 bytes, as exemplified in the first scenario depicted in Fig. 1.

This contribution places a specific emphasis on achieving precise synchronization, particularly within distributed systems where multiple remote entities necessitate synchronous action. Notably, the current operational paradigm relies exclusively on a hardware-based mechanism for EtherCAT data exchange.

Given that communication in this context adheres both logically and physically to the daisy-chain structure, the master clock assumes the role of determining propagation delays and offsetting slave clocks in a direct and precise manner. The synchronization accuracy is thereby attainable at a level below one microsecond.

In terms of practical application, the generation of SYNC0/1 and LATCH0/1 signals [20] via Interrupt ReQuest (IRQ) events holds paramount significance as it triggers network operations and timestamps saving, subsequently leading to a substantial reduction in latency. These signals can be directed to external Input/Output (I/O) pins within the Electronic Slave Controller (ESC) hardware.

The full-duplex connection is consistently supported between two ESC ports, as stipulated by the EtherCAT Technology Group (ETG). A "segment" is defined as a collection of n ESCs linked to one or more ESCs, and it maintains a logical ring topology, even within a daisy-chain configuration. As illustrated in Fig. 2a, the n^{th} slave is responsible for processing and forwarding frames via the four ports outlined in Fig. 2b. The number of ports is ESC-specific, with each ESC in the paper's setup accommodating four ports. The EtherCAT Processing Unit (EPU) within the ESC embeds and processes incoming frames solely from the IN port, referred to as the processing direction. Other directions are considered forwarding directions. Frame processing within the EPU encompasses datagram handling, auto-forwarding/loop-back functionality, and Fieldbus Memory Management Unit (FMMU) operations.

In terms of shared memory functionality, the Sync-Manager (SM) and FMMU play pivotal roles in facilitating data exchange between the master and ESCs. When communication between the master and slaves occurs in an acyclic fashion, the SM operates in one-buffer mode; otherwise, it operates in three-buffer mode. In the current scenario, the SM serves exclusively for memory sharing, with Distributed Clock (DC) handling the synchronization process.

In DC mode, there are three distinct settings: (1) Master Shift (MS), where the local clock of the first slave is utilized to readjust the master timer; (2) Bus Shift (BS), where the master retains control over time and configures it for the first slave; and (3) the utilization of an external reference clock, such as a global time system, across all devices. The current setup adheres to the first DC mode, the Master Shift (MS). The master shift is the offset in time between the start of the CT and the actual transmission of the EtherCAT frame, accounting for software or synchronization-related delays.

Upon the processing and routing of frames through both frame processing and forwarding paths, the frame delay can be estimated in accordance with (1). $T_{\text{FrameDelay}}$ represents the minimal achievable Cycle Task (CT), with any delays incurred being proportional to $T_{\text{FrameDelay}}$. In this study, we set the CT to 5 ms, a choice contingent on the CPU performance of the master when operating in DC mode. It is imperative to ensure that the CT does not surpass the global clock performance of the master's CPU, as exceeding this threshold would result in frame drops and a loss of DC synchronization.

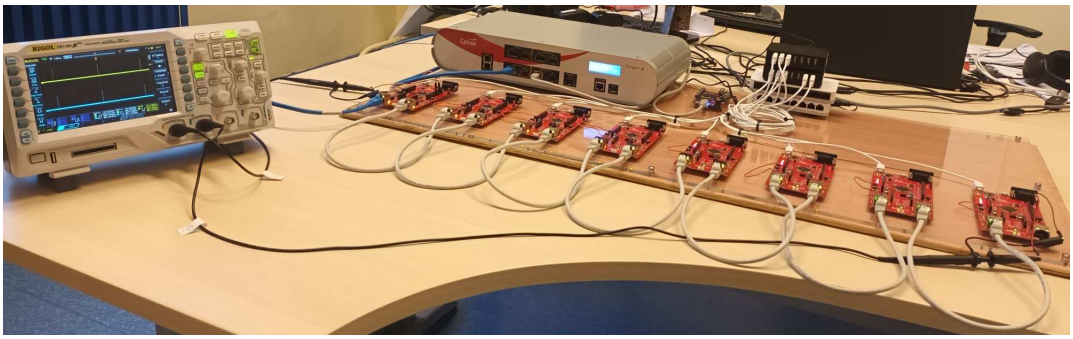
III. System setup

To experimentally investigate the synchronization and latency characteristics under realistic conditions, we implemented a complete EtherCAT network prototype. The following section details the system setup, including hardware components, network configuration, and the open-source tools used in the evaluation.

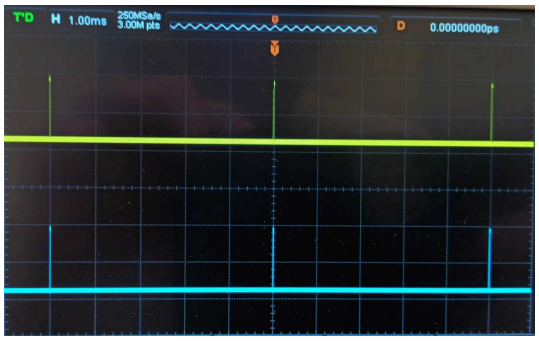
A. Open Source IgH EtherCAT Master

Fig. 3d elucidates the architectural framework of the IgH master, with reference to prior research contributions [21]–[23]. The diagram's constituent blocks, numbered from 1 to 6, are delineated as follows:

① The slave entities offer their inputs and outputs by presenting Process Data Objects (PDOs) to



(a)



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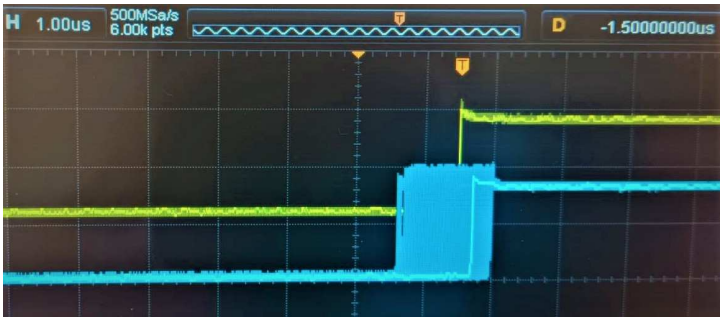

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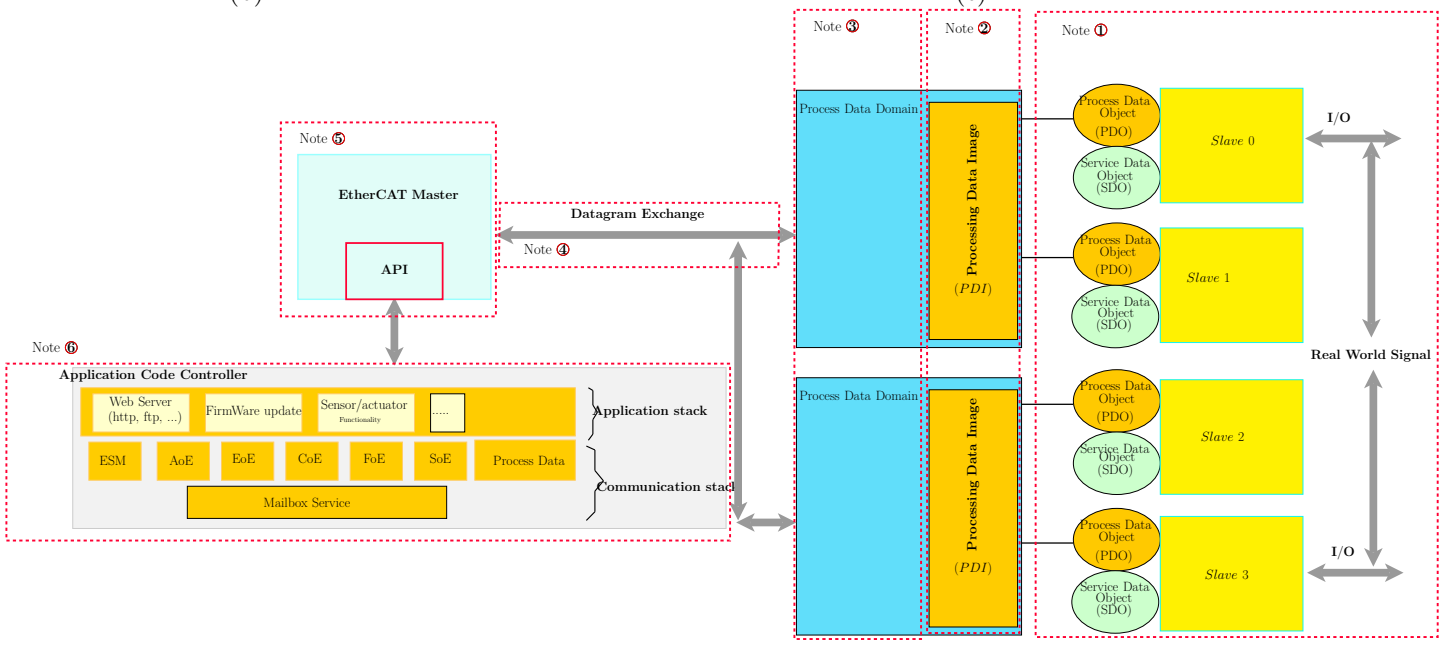


(d)

Figure 3: (a) Experimental setup showing a packet analyzer connected in-line with eight EtherCAT slaves via 100 Mbps Ethernet (blue cable, left) and an IgH EtherCAT master via 100 Mbps Ethernet (white cable, right). Two oscilloscope probes are connected to digital I/Os on the 1st and 8th slaves to monitor synchronization behavior. (b) Oscilloscope capture displaying interrupt output signals from the 1st and 8th slaves. (c) Zoomed view of the oscilloscope output, revealing a registered synchronization delay of 1.5 µs. (d) Illustration of communication and interaction processes between the IgH EtherCAT master and the connected slave devices.

the master. The determination of available PDOs can be accomplished by reading the TxPDO categories or RxPDO via the Electrically-Erasable Programmable Read-Only Memory (E2PROM) shared memory. Additionally, Service Data Object (SDO) functionality is commonly available on most slaves to facilitate task-specific maintenance procedures.

(2) The application has the capacity to store the inputs associated with the PDOs designated for exchange during cyclic operations. The Processing Data Image (PDI) is defined as the aggregate of all subscribed PDO entries. The data transferred between these PDIs is managed through datagrams featuring logical memory access, such as Logical Memory Write (LWR), Logical Memory Read (LRD), or Logical Memory Read-Write (LRW).

(3) Domains are established to facilitate communication among groups of PDOs, with a minimum of one domain being requisite for data processing.

(4) Datagrams can be interchanged at varying rates for each domain, allowing for flexibility in data exchange.

(5) The master module exclusively operates within the kernel space and can accommodate multiple masters within its module. It exhibits compatibility with a spectrum of real-time Linux extensions, owing to its autonomous architecture. In the present configuration, the RT-Preempt kernel Linux patch is adopted, aligning seamlessly with the EtherCAT master employed, which relies on Sitara hardware CPU technology developed by Texas Instruments.

(6) The application can reside either within the kernel space or user space via the Application Programming Interface (API). The EtherCAT master facilitates the use of the Ethernet over EtherCAT (EoE) mailbox protocol, enabling the tunneling of Ethernet frames to specific slaves, which may possess physical Ethernet ports or incorporate their IP stack to receive such frames. Furthermore, the CANopen over EtherCAT (CoE) protocol serves to configure slaves and facilitate data object exchanges at the application level. The Vendor-specific over EtherCAT (VoE) protocol offers the means to implement vendor-specific mailbox communication protocols. Lastly, the Servo Profile over EtherCAT (SoE) protocol allows for the realization of the service channel layer via EtherCAT mailboxes.

The master module disseminates information pertaining to its status and events through the kernel ring buffer, and these details are also recorded in the system logs.

B. Experimental Setup

Table II: Hardware Master Specifications of IgH

Hardware module	**Specifications**
Processor	-TI Sitara AM3359 -ARM Cortex A8 -1 GHz
RAM	-512 MB DDR3
Power	5 V
Connectivity	-One USB Host -One Mini-USB Client -One 10/100 Mbps Ethernet port
Storage	-2 GB onboard eMMC -1 MicroSD

As depicted in Fig. 3a, the experimental configuration comprises eight Electronic Slave Controllers (ESCs) interconnected in a daisy-chain topology. A packet analyzer is introduced into this setup, serially connected via a 100 M Ethernet blue cable, extending from the left side to the IgH master situated on the right side. The role of the packet analyzer is to record, at the second layer of the OSI model, the time delays encompassing the entire Ethernet packet, which encapsulates 1486 bytes of EtherCAT frame data. These packets are transmitted from the 8^{th} ESC to the IgH master. The hardware specifications of the IgH master are delineated in Tab. II. It is noteworthy that the processor clock frequency and the capacity of Random Access Memory (RAM) play a pivotal role in determining the minimum cycle task period.

The oscilloscope serves as a critical tool for capturing signals generated by SYNC0, identifiable by a specific I/O pin originating from both the 1^{st} ESC (indicated by the yellow signal) and the 8^{th} ESC (represented by the blue signal) in Fig. 3b and Fig. 3c. It is important to note that these signals can only be effectively captured when the Distributed Clock (DC) mode is activated.

Figure 1b illustrates that the signals received at the oscilloscope's probes exhibit strong synchronization; however, for a more accurate assessment of synchronization precision, refer to Figure 1c.

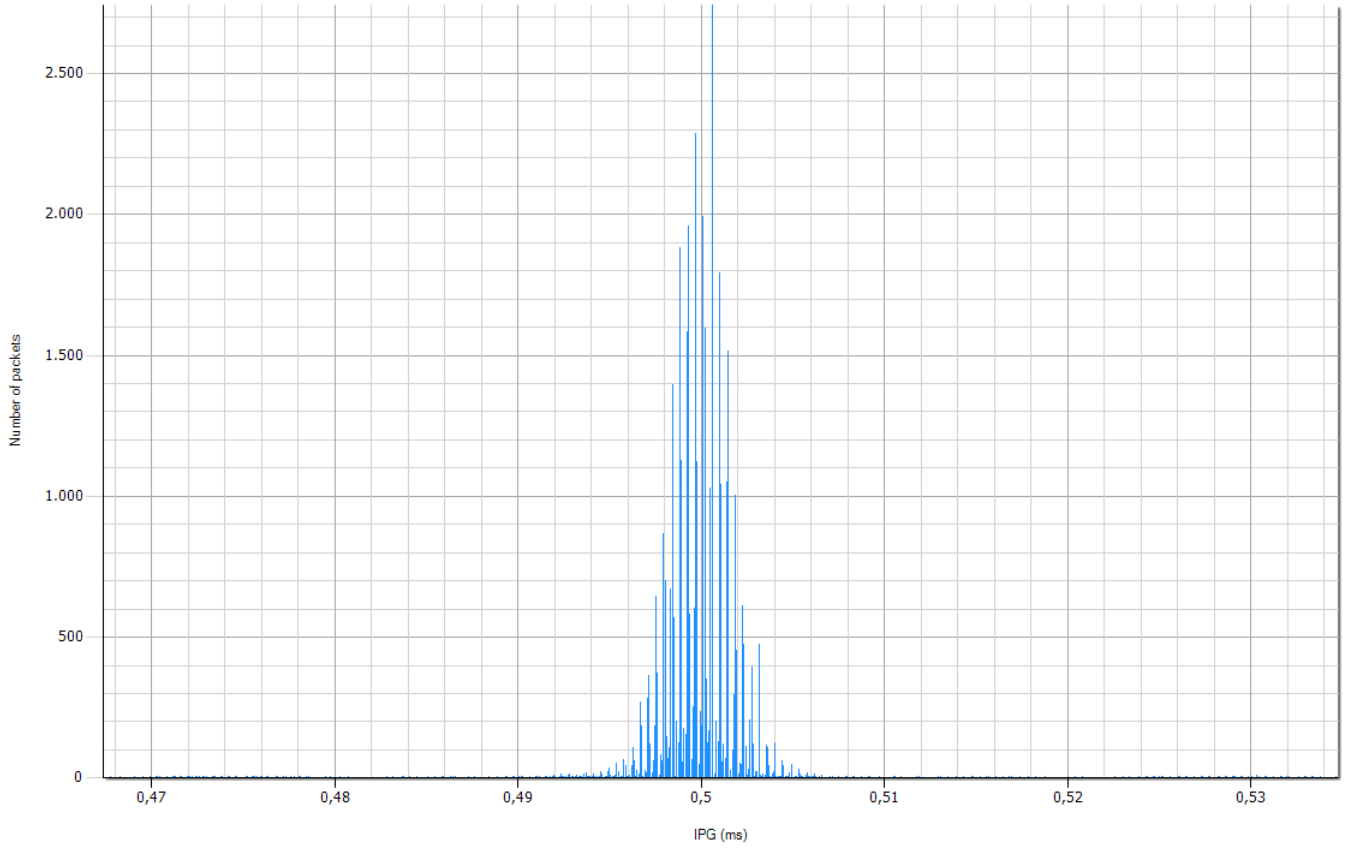


Figure 4: Packet Delay Distribution (PDD) illustrated as : Number of Packets (1518 bytes) with respect to Inter-Packet Gap (IPG) registered by the packet analyzer (mean=0.5 ms, min=0.467 ms, max=0.535 ms)

Quantitative measurements indicate a delay of 1.5 µs at the physical layer, as recorded by the oscilloscope's probes. Additionally, an Inter-Packet Gap (IPG) of 0.5 ms, observed at the second layer of the OSI model using the packet analyzer, is evident (as depicted in Fig. 4). It is crucial to distinguish IPG from jitter or frame delays, as IPG represents a latency interval imposed by the IEEE 802.3 standard to facilitate timing recovery at the receiver side, and should not be conflated with other timing variations or frame delays.

IV. Experimental Measurement Analysis

Having outlined the system components and configuration, we now focus on the experimental measurements, detailing the tools, metrics, and procedures employed to quantify performance across multiple network layers.

Time delays are readily accessible and extractable from the IgH master dashboard through the Application Programming Interface (API). A shell script was developed to systematically gather these time delays, achieving a granularity as fine as nanoseconds.

Fig. 6a visually presents the compiled time delay data gathered over a duration of 10 min. This experiment underwent eight repetitions, with each iteration corresponding to a specific order of Electronic Slave Controllers (ESCs) within the daisy-chain, where the delay measurement was conducted. In this configuration, the maximum recorded delay, observed under worst-case conditions, approximates 1.6×10^5 nanoseconds (ns), while the minimum delay, occurring under the most favorable circumstances, is approximately 0.8×10^5 ns. An apparent variation in the establishment periods of the ESCs is discernible, a characteristic that can be adjusted through the chosen Master Shift (MS) mode.

Fig. 6b presents statistical insights derived from the measured delays, encompassing standard deviation and mean values for each measurement.

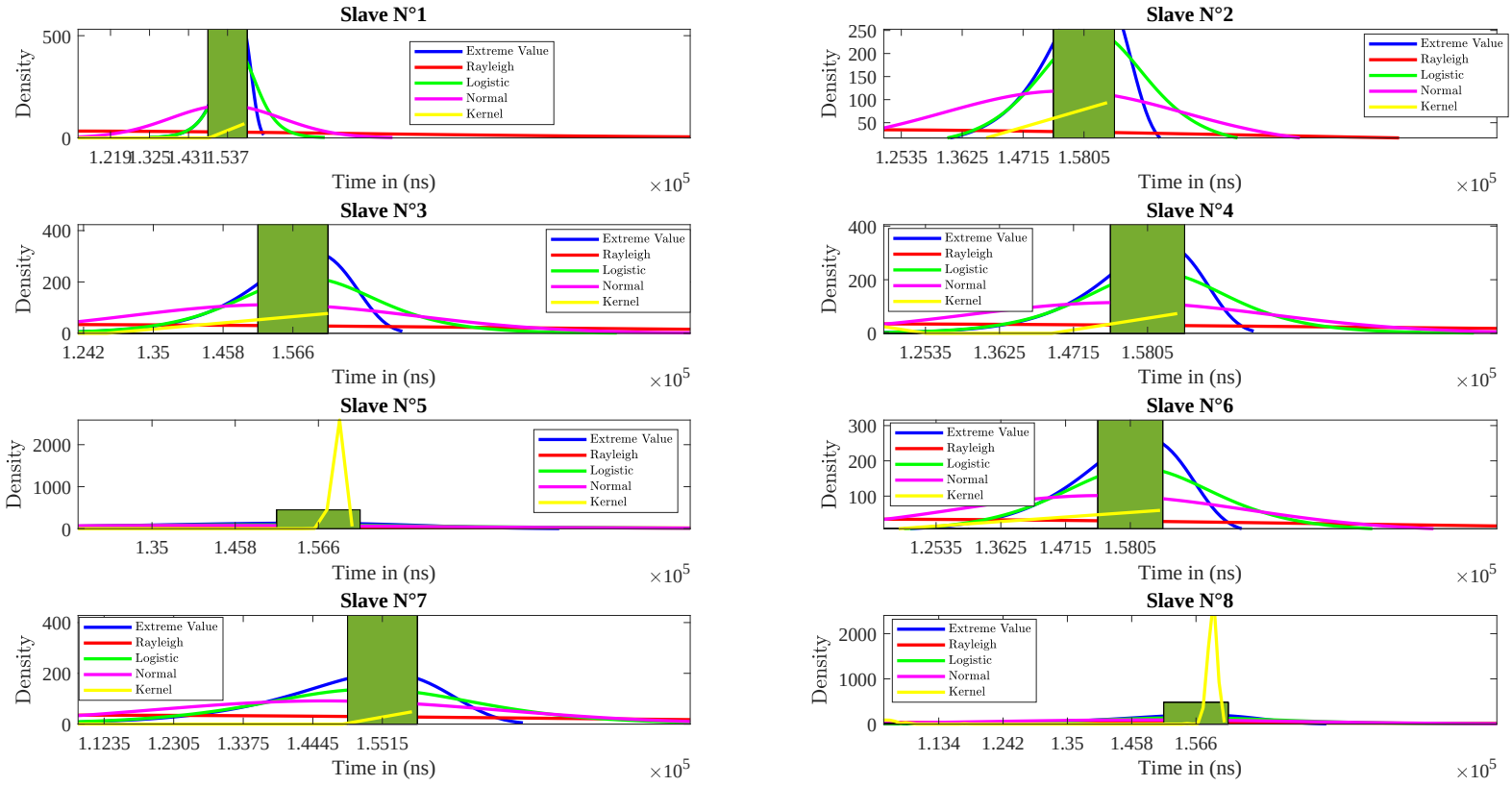


Figure 5: The logistic statistical model was evaluated against four alternative statistical distribution models to assess its relative performance and goodness-of-fit

Meanwhile, Fig. 6c exhibits the response profile of a proposed S-function when applied to elapsed time.

A. S-function Approximation

Fig. 6c reveals a distinct characteristic in the relationship between the acquired time delays and the corresponding elapsed time, manifesting an "S"-shaped curve. This particular curve conforms to an S-function, often referred to as the sigmoid function, which can be represented mathematically as $\frac{\alpha}{1+\exp(-x)}$, where x signifies the recorded elapsed time. The discerned curve closely resembles the pattern observed in Fig. 6a, consolidating the findings presented in Fig. 5

In our pursuit of identifying an appropriate statistical model to encompass the current results, we posit that the logistic law may offer a fitting framework. This assertion is rooted in the observation that the S-function typically aligns with data-sets that conform to logistic regression principles [24]. We observed that the latency over time exhibited a nonlinear, saturating growth pattern, reminiscent of a sigmoidal curve. Given this behavior, often associated with feedback-limited or resource-constrained systems, we hypothesized that a logistic model could effectively capture the dynamics. To further substantiate this hypothesis, we subjected the obtained time delays to four distinct candidate laws: Extreme Value, Rayleigh, Normal, and Kernel. The results, as depicted in Fig. 5 suggest that the logistic law is a suitable choice for the majority of ESCs, with the exception of the 8^{th} and 5^{th} ESCs. Armed with this dual-pronged approach, we contend that the time delays likely adhere to the logistic law.

B. Logistic regression

Building upon the conclusions drawn in Subsection IV-A, it is possible to depict the behavior

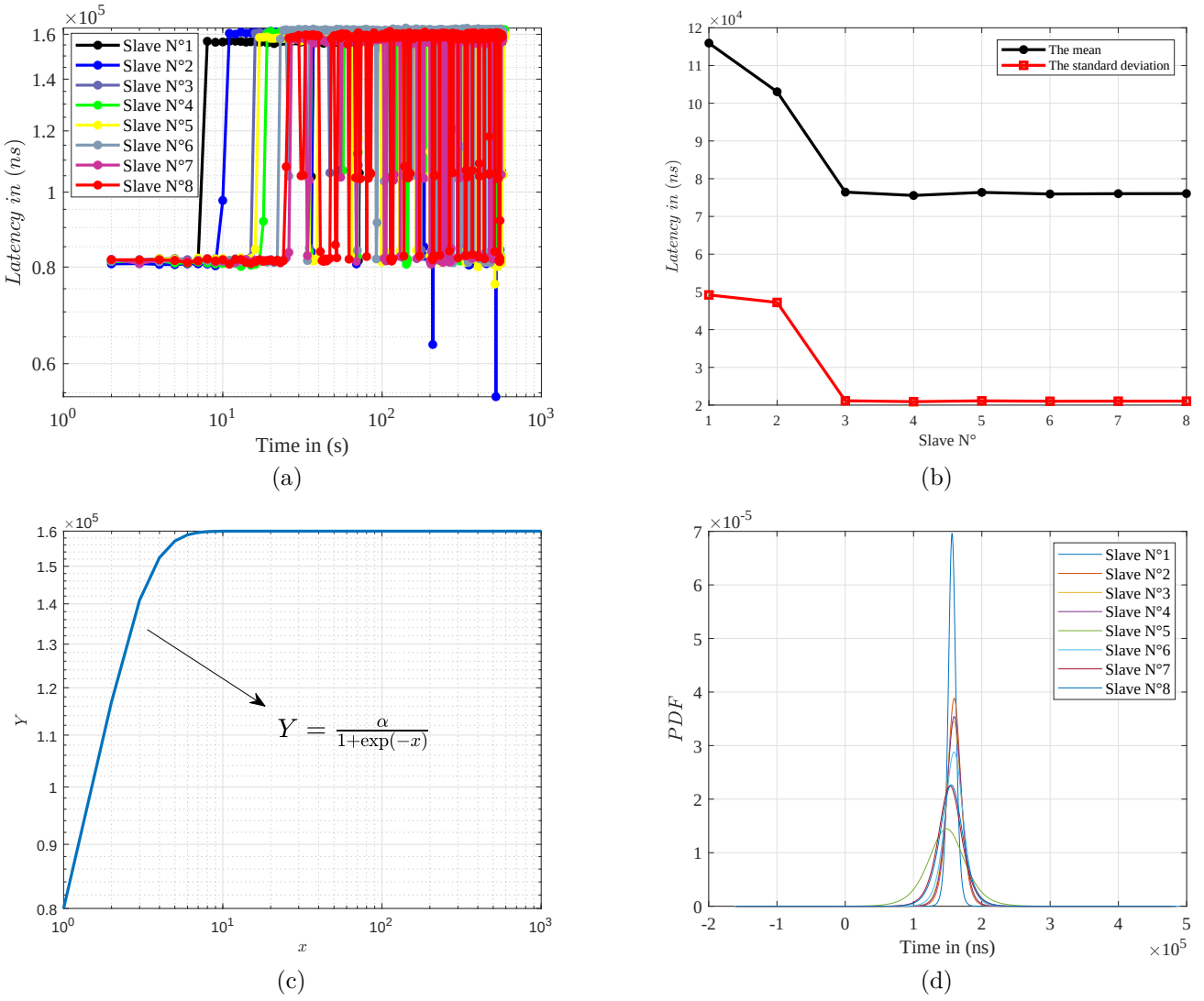


Figure 6: (a) Experimental delay measurements extracted using the Linux OS diagnostic dashboard and the IgH EtherCAT master tool, with the Distributed Clock period set to 5 ms. (b) Mean and standard deviation of the measured latency values across multiple runs. (c) Representative example of an S-function used for modeling or control integration within the test environment. (d) Statistical analysis based on the logistic distribution, showing the relationship between fitted parameters and the number of EtherCAT slave nodes.

of the logistic law across all Electronic Slave Controllers (ESCs), as exemplified in Fig. 6d. Notably, as the number of ESCs within the daisy-chain configuration increases, the Probability Density Function (PDF) profile assumes a less flattened shape, resulting in time delays clustering closer to the mean value.

To facilitate a more explicit examination of the mean and standard deviation values emanating from the logistic laws illustrated in Fig. 6d, we have introduced Table. IIIa. The mean values exhibit a range spanning from 1.5528×10^5 to 1.5640×10^5 ns.

When applying the 3σ (3-sigma) rule to the worst-case scenario documented in Table. IIIa, it becomes evident that 68.27% of time delays fall within the interval $[1.5281 \times 10^5 \ldots 1.5999 \times 10^5]$ ns, 95.45% of time delays reside within the range $[1.4922 \times 10^5 \ldots 1.6358 \times 10^5]$ ns, and 99,73% of time delays are encompassed within the span $[1.4563 \times 10^5 \ldots 1.6717 \times 10^5]$ ns.

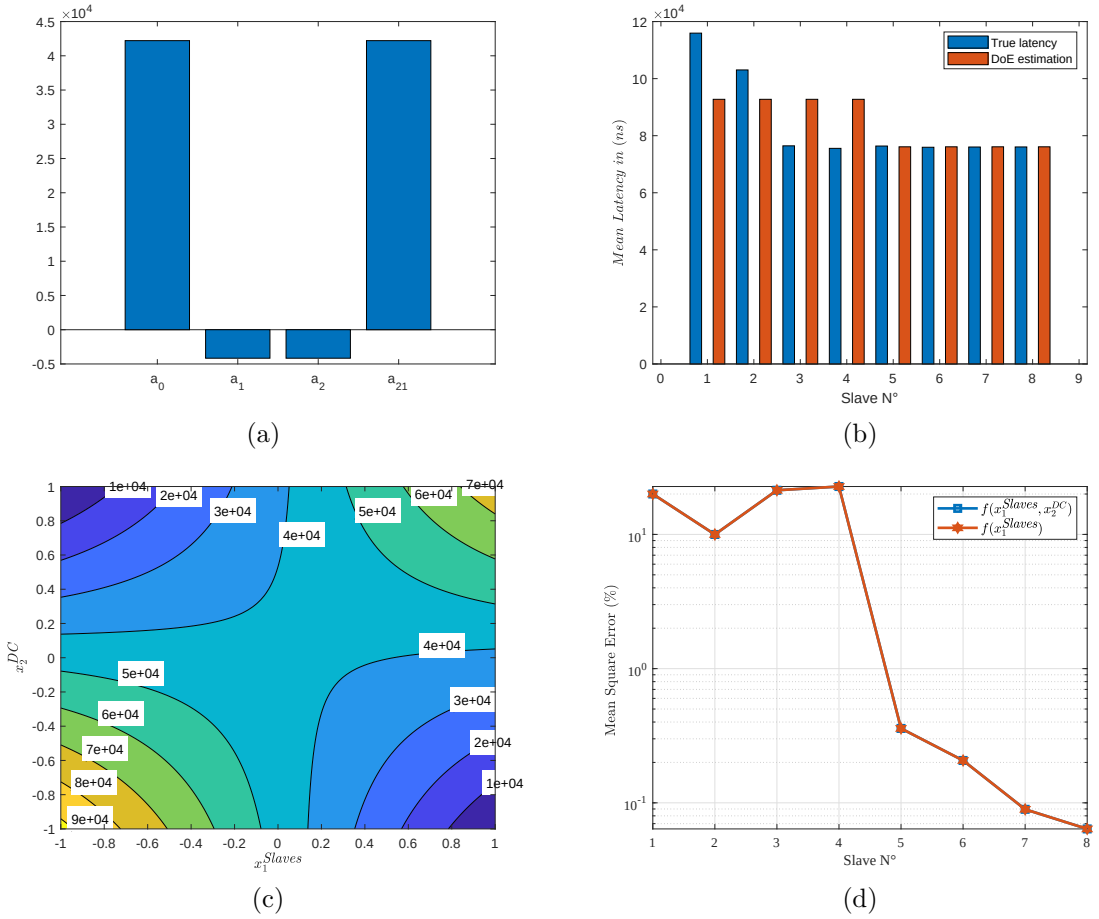
Table III: (a) Statistics issued from Logistic law analysis $(\mu, \sigma, 3\sigma)$ based on Fig. 6d. (b) ANOVA Analysis.

Slave's order	**1**	**2**	**3**	**4**	**5**	**5**	**7**	**8**
μ (ns)	1.5528×10^5	1.5340×10^5	1.5937×10^5	1.4824×10^5	1.5949×10^5	1.5893×10^5	1.5957×10^5	1.5640×10^5
σ(ns)	1.1037×10^4	1.1125×10^4	0.8676×10^4	1.7285×10^4	0.7056×10^4	0.7237×10^4	0.6439×10^4	0.3590×10^4
$\mathbf{3}\sigma$(ns)	3.3112×10^4	3.3374×10^4	2.6027×10^4	5.1855×10^4	2.1168×10^4	2.1711×10^4	1.9316×10^4	1.0771×10^4

(a)

Source	**Degree of freedoms**	**Sum of the mean square errors**	***p*-value**
x_1^{Slaves}	10	8.38×10^7	0
x_2^{DC}	10	1.92×10^{-57}	1
$x_1^{Slaves} \times x_2^{DC}$	10	1.025×10^{-23}	1

(b)



(a) (b) (c) (d)

Figure 7: (a) Coefficient weights of the response variable $Y = f(x_1^{Slaves}, x_2^{DC})$ prior to ANOVA analysis, illustrating the influence of each factor on the model. (b) Estimation accuracy of latency using the Design of Experiments (DoE) methodology, showing results before and after ANOVA analysis for comparison. (c) Contour plot depicting the topology of the factor pair (x_1^{Slaves}, x_2^{DC}), highlighting interaction effects. (d) Comparison of DoE results with actual latency measurements, validating the predictive accuracy of the model.

V. Latency Modeling with DoE Methodology

While the latency model and DoE analysis provide a structured understanding of parameter ef-

fects, empirical measurements are essential to confirm theoretical insights. The subsequent section presents the experimental results obtained from our testbed.

To go beyond traditional empirical benchmarking, this work integrates a Design of Experiments (DoE) framework into the EtherCAT system evaluation pipeline. Unlike previous studies that often rely on heuristic or fixed-parameter measurements, our approach systematically explores the design space by varying key configuration parameters such as distributed clock synchronization modes, cycle task intervals, and the number of EtherCAT slaves. This allows for a quantitative modeling of latency behavior, revealing statistically significant interactions between protocol-level settings and synchronization performance.
Furthermore, the experimental system is deliberately built using open-source EtherCAT master stacks (IgH), which, when combined with low-level measurements at the Media Independent Interface (MII) level, enables fine-grained access to PHY-layer delays-an often overlooked but critical dimension in time-sensitive industrial applications.

To the best of our knowledge, this is the first publicly documented methodology that combines DoE-based statistical analysis with hardware-level timing validation under MII-based EtherCAT configurations, thereby offering a replicable and extensible framework for performance evaluation in real-time Ethernet systems.

The Design of Experiment (DoE) methodology, as outlined in references [25], [26], serves as a systematic approach for the development of predictive models that elucidate trends within systems. These models are adept at forecasting system responses contingent upon their constituent parameters, referred to as "factors." The foundation of these models rests upon empirical data obtained from experiments, which subsequently undergo rigorous statistical analysis. Importantly, the DoE-driven model dispenses with the necessity for fundamental analysis of underlying phenomena, devoid of any inherent physical interpretation. Within this framework, "controlled factors" denote parameters with the potential to exert influence on the outcomes of an experiment, while all other factors are designated as "uncontrolled factors." The spectrum of values that a controlled factor can assume is referred to as "levels," and the model's response materializes as a numerical result generated during an experimental trial, contingent upon a specific treatment. The extent of a factor's impact on the response is termed the "effect." There are two discernible categories of effects: "main effects," which embody the direct influence stemming from a controlled factor, and "interactions effects," which encompass the effects resulting from the interplay between factors, often referred to as "second-order interactions."

A. Problem Definition

In this work, we spotted two essential factors that could impact the time delays: the number of slaves ESCs, and the Cycle Task (CT) periods used by the DC. The factors (x_1^{Slaves}, x_2^{DC}) will shape the design of the plan as follow:

$$\begin{aligned} Y &= f(x_1^{Slaves}, x_2^{DC}) \\ &= a_0 + a_1 x_1^{Slaves} + a_2 x_2^{DC} + a_{12} x_1^{Slaves} x_2^{DC} \\ x_1^{Slaves} &= \text{Slave orders} \in [1, 8] \\ x_2^{DC} &= \text{DC values} \in [1, 5] \text{ ms} \\ Y &= \text{The mean latency per trial} \end{aligned} \tag{2}$$

Matrix (3) summarizes the DoE model of (2):

$$\left(\begin{array}{cccc} \textbf{Trial} & x_1^{Slaves} & x_2^{DC} & Y \\ \hline 1 & - & - & y_1 \\ 2 & - & + & y_2 \\ 3 & + & - & y_3 \\ 4 & + & + & y_4 \\ 5 & - & - & y_5 \\ 6 & - & + & y_6 \\ 7 & + & - & y_7 \\ 8 & + & + & y_8 \\ \hline - & \min = 7\,\text{ms} & \min = 1\,\text{ms} & \\ + & \max = 8\,\text{ms} & \max = 5\,\text{ms} & \end{array}\right) \tag{3}$$

B. Preliminary Results

Following the mathematical manipulation of equations (3) and (2) to determine the values of a_i, a_{ij}, the function $f(x_1^{Slaves}, x_2^{DC})$ attains complete definition. In accordance with the observations gleaned from Fig. 7a and Fig. 7b, it becomes evident that an increase in the number of slaves contributes to enhanced precision in the DoE estimator. Fig. 7c presents a contour topology of the

parameter pair (x_1^{Slaves}, x_2^{DC}), providing a visual representation of the variations in $f(x_1^{Slaves}, x_2^{DC})$ while x_1^{Slaves} across the range of x_1^{Slaves} concerning x_2^{DC}.

C. ANOVA Optimization

In pursuit of enhancing the optimization of the results outlined in Subsection V-B, we employed the Analysis of Variance (ANOVA) methodology. Typically, ANOVA encompasses an array of estimation tests designed to evaluate the impact of controlled factors and their interrelations.
To this end, we introduced the concept of the p-value in Tab .III(b), which serves as a quantitative indicator of the factor's significance within the proposed model. As the p-value approaches zero, it signifies a noteworthy level of significance, indicating the substantial influence of the factor on the model. Conversely, when the p-value deviates from zero, it suggests that the factor exerts minimal influence on the model's behavior.
Upon subjecting the ANOVA test to scrutiny, it becomes evident that only x_1^{Slaves} merits inclusion within the model. This assertion finds validation through the juxtaposition of the reduced model with the actual measurements, as illustrated in Figure Fig. 7d.

D. Summarize of the obtained results

To more clearly present these findings, we summarize the key advancements as follow:

- **Minimalist hardware setup with high-resolution insight:**

Unlike many prior studies that rely on complex or specialized proprietary hardware and software (e.g., TwinCAT 3) to be used as Master controller, our measurements were conducted with an open-source Master installed on a resource-constrained embedded platform (BeagleBone Black). Despite hardware limitations, we achieved precise delay measurements using lowd-level monitoring via the MII interface. This demonstrates the feasibility of ultra-low latency EtherCAT systems (1.5 ms) on minimal hardware-a highly valuable result for cost-sensitive industrial deployments.

- **Statistical modeling of delay profile:**

Through extensive latency measurements, we identified that the logistic distribution best fits the observed EtherCAT delay profile. The probability density function (PDF) used is:

$$f(x;\mu,\tau) = \frac{e^{-\frac{x-\mu}{\tau}}}{\tau\left(1+e^{-\frac{x-\mu}{\tau}}\right)^2} \tag{4}$$

where μ is the mean delay and τ is the scale parameter. This model allows system designers to predict latency distribution across nodes and scenarios.

- **Latency bounds via 3σ rule:**

Using the fitted logistic model, we applied the **3σ rule** to derive an interval of confidence $(\mu \pm 3\sigma)$, which encapsulates 99.7% of delay occurrences. This is highly relevant for real-time applications, as it quantifies the safe operating window for deterministic communication.

- **Latency predictability across node chains:**

The model enables analytical prediction of end-to-end delay as a function of the order of EtherCAT slaves ,n, where delay growth is shown to be linear: $D(n) = a_0 + a_1 x_1^{Slaves}$

- **DoE and ANOVA analysis confirm parameter independence:**

We performed a Design of Experiments (DoE) study and used ANOVA to evaluate the effects of Distributed Clock (DC) and Cycle Task (CT) configurations. The p-values for interaction terms exceeded 0.05, indicating no statistically significant impact or interaction on delay performance. This insight streamlines configuration efforts for EtherCAT integrators.

- **Record-level delay at PHY layer:**

To our knowledge, this is the first study reporting a 1.5 µs PHY-layer delay using open-source IgH master and standard Ethernet cabling, confirmed by time-synchronized oscilloscope measurements. This sets a new benchmark for real-time industrial networking performance using open and accessible tools.

VI. Conclusions

This study provides a comprehensive analysis of EtherCAT network performance, focusing on latency and robustness under synchronized communication loads, with an emphasis on the use of MII connections and an open-source master. The

proposed methodology, which integrates experimental design (DoE) and detailed latency modeling, demonstrates significant improvements in the understanding of real-time communication in industrial networks. Specifically, we identified critical latency thresholds at various layers, including the PHY layer, which is crucial for time-sensitive applications.

The customized experimental setup yielded noteworthy findings, including the achievement of an inter-packet gap of 0.5 ms at the packet layer, 1.5 ms at the frame layer, and 1.5 µs at the physical layer, particularly when employing the DC mode with master shift configuration. Ultimately, the investigation into the extrapolated time delays, facilitated by an open-source IgH master, and culminated in the identification of a logistic law profile, serves as a robust statistical framework, offering a straightforward parameterizations to characterize the observed statistical properties effectively. The findings of this study can be directly applied to several industries that rely on real-time Ethernet-based communication, including industrial automation, robotics, and process control. The ability to optimize synchronization in EtherCAT networks will enable the development of more responsive and reliable control systems. The use of open-source tools provides a cost-effective, accessible solution for practical implementations, which could significantly benefit small and medium-sized adopting EtherCAT for automation systems.

By employing the Design of Experiments (DoE) methodology, this research also offers a replicable framework that can be adapted to other network configurations and communication protocols, further extending the scope of its applications in industrial settings. The proposed approach not only advances the understanding of EtherCAT performance but also lays the groundwork for future innovations in real-time industrial networking. These results contribute also to the ongoing efforts to integrate industrial Ethernet, within emerging 5G/6G communication infrastructures. Time-Sensitive Networking (TSN) stands out as a key enabler by providing deterministic guarantees and enabling synchronization across heterogeneous networks. The latency modeling supports this by offering precise bounds on wired communication delays. This can facilitate harmonization between wireless (5G/6G) and wired (EtherCAT) timing domains. Additionally, there is room to extend our current setup toward hybrid architectures by adapting EtherCAT for Wi-Fi 7, leveraging its low-latency and deterministic capabilities. This direction opens promising opportunities to widen the applicability of EtherCAT in flexible and wireless industrial scenarios.

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