A method for designing high-frequency operational amplifiers using the g_m/I_d methodology

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Introduction

Operational amplifiers are one of the most used devices in analog electronics. Even accounting with a vast know-how on analog design, the design of such circuits is time-consuming. The main idea behind this project consists in developing a design methodology that allows to save time at the design phase. As a proof of concept we have chosen an HF application, which are well-known because of the difficulty to achieve the target specifications by means of traditional design. We first chose the op amp topology and then built its high-frequency model. To design our amplifier we used the so-called "g_m/I_d methodology" [1], which is based on the universal transconductance-to-current ratio of the MOS transistor. Finally, we simulated the circuit with CADENCE SPECTRE.

1. Specifications

Four main specifications:

1. f_T = unity-gain frequency > 500 MHz (target = 1 GHz);
2. Ao = open-loop DC gain > 60 dB
3. PM = phase margin > 45 ° (target = 60 °);
4. CL = load capacitance = 1-2 pF.

2. Topology

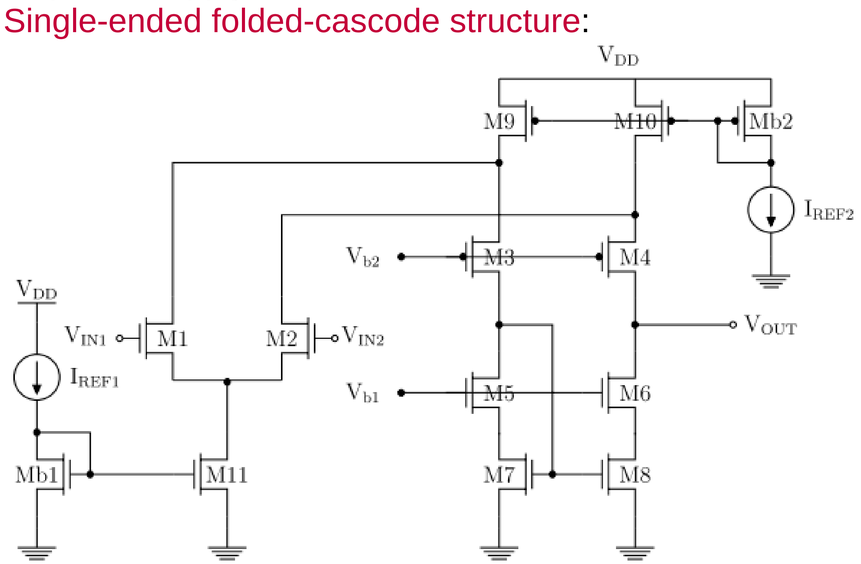
Folded-cascode / gain-boosted op amp:

On the one hand, we need a high-speed operational amplifier. So we have to use minimum transistor's size in order to decrease junctions capacitances. But this implies higher drain-to-source voltages and thus lower signal swing. This leads to choose a folded-cascode architecture [2]. On the other hand, we need a high-gain amplifier. In this case, the gain-boosted cascode topology is more appropriate. We have studied both topologies and chosen the best trade-off.

Single-ended VS fully-differential:

- **fully-differential** = best performances in terms on bulk noise and power supply rejection. Need of an extra CMRR circuit to set the outputs DC level of the op amp.
- **single-ended** = easier to design but more prone to noise and power supply variations effects.

Single-ended folded-cascode structure:



3. g_m/I_d methodology

Steps:

1. High-frequency model (more or less accurate).
2. Poles and zeros, DC gain, Impedances: parametrical characterization by means of the g_m/I_d of the involved transistors.
3. Parameters computation (PM, f_T…).
4. SPECTRE simulations using the BSIM4 model.

Example:

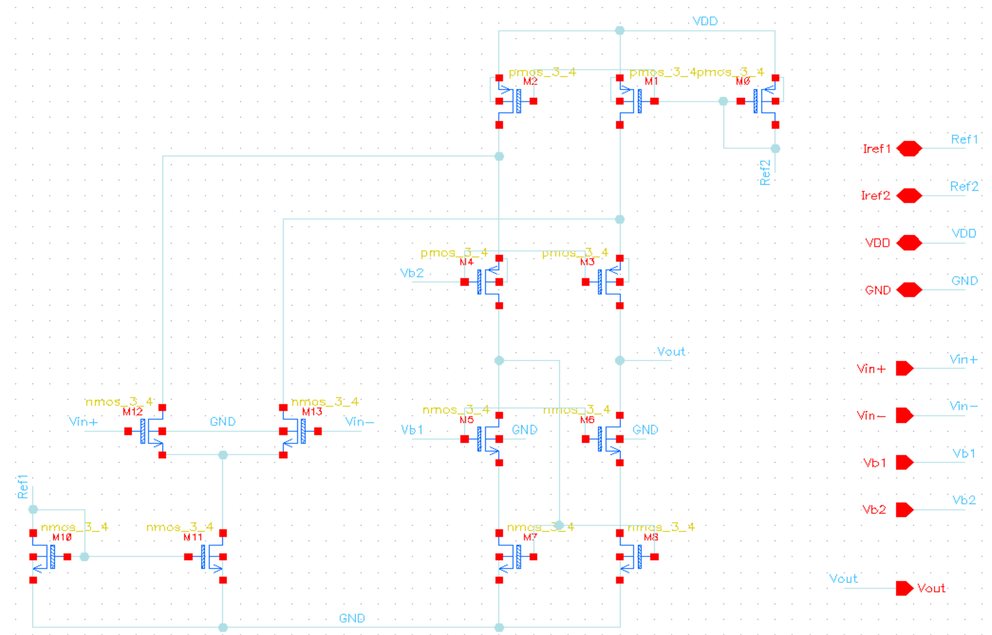
$$\omega_{OUT} = \frac{1}{R_{OUT}\,C_{OUT}} \qquad R_{OUT} = \frac{(g_{m_4}\cdot r_{0,4})\cdot\frac{r_{0,10}\cdot r_{0,2}}{r_{0,10}+r_{0,2}}\cdot(g_{m_6}\cdot r_{0,6})\cdot r_{0,8}}{(g_{m_4}\cdot r_{0,4})\cdot\frac{r_{0,10}\cdot r_{0,2}}{r_{0,10}+r_{0,2}}+(g_{m_6}\cdot r_{0,6})\cdot r_{0,8}} \qquad C_{OUT} = C_{load} + C_{DB_{M4}} + C_{DB_{M6}}$$

$$\omega_{OUT} \approx \frac{1}{C_{load}+(S_{M4}+S_{M6})\cdot(C_j+2\,C_{jsw})}\cdot\frac{\delta\cdot\left(\frac{g_{m_4}}{I_{D_4}}\right)\cdot I_{D_4}+\varepsilon\cdot\left(\frac{g_{m_6}}{I_{D_6}}\right)\cdot I_{D_6}}{\iota\cdot\left(\frac{g_{m_4}}{I_{D_4}}\right)\cdot I_{D_4}\cdot\left(\frac{g_{m_6}}{I_{D_6}}\right)\cdot I_{D_6}}$$

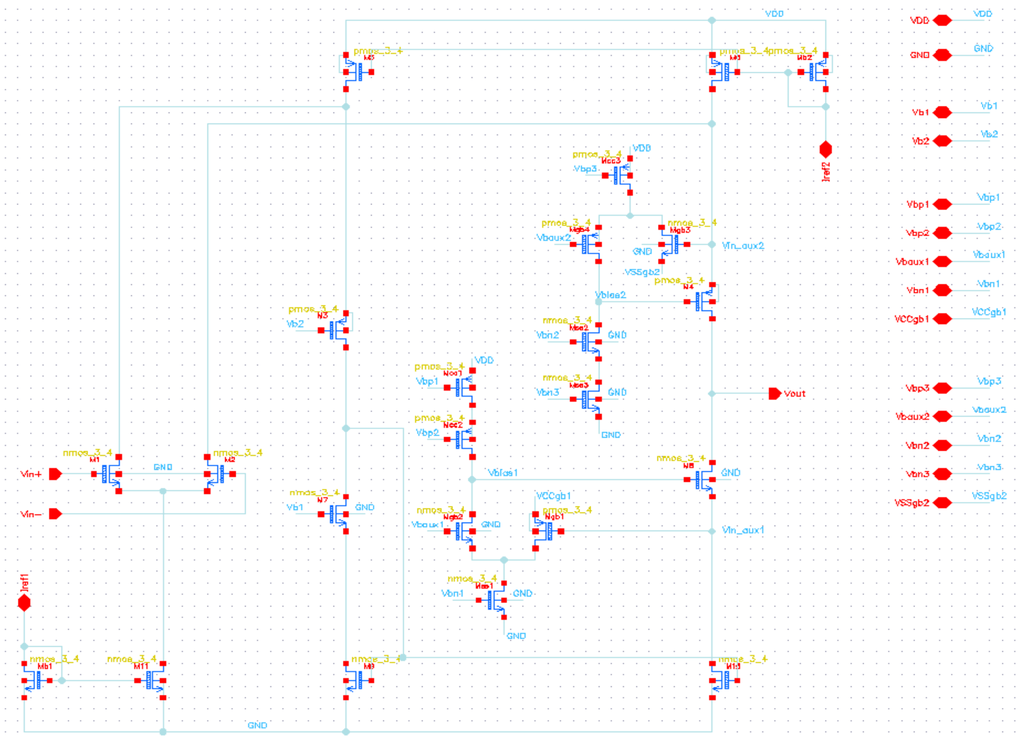
$$\delta = r_{0,2}\cdot r_{0,4}\cdot r_{0,10},\quad \varepsilon = (r_{0,6}\cdot r_{0,8})\cdot(r_{0,2}+r_{0,10}),\quad \iota = \gamma\cdot\delta = r_{0,2}\cdot r_{0,4}\cdot r_{0,6}\cdot r_{0,8}\cdot r_{0,10}.$$

4. Circuits schematics

Folded-cascode



Gain-boosted



5. Results

Voltage supply = 1.8 V.
Technology = Lfoundry 150nm.

Amplifier	DC gain [dB]	Unity-gain freq [Hz]	Phase margin [°]
Folded-cascode:	38.4	877.8 M	48.02
Gain-boosted:	62	937.2 M	41.77

How to achieve better results?

1. Using more accurate models (EKV or ACM models) at the hand calculations steps.
2. Running optimization procedures in closed-loop that make use of classic optimization algorithms.

Conclusion

In this work we used the g_m/I_d methodology to design an amplifier targeting high frequency applications. We proposed a design method, which consists in choosing the amplifier topology according to the specifications and then building its high-frequency model. Based on this model, one can parameterize poles, zeros, DC gain, f_T as well as nodes impedances by means of the g_m/I_d of transistors. Thanks to this, we can predict amplifier parameters, like the phase margin or the unity-gain frequency, before simulations. With a very simple high-frequency model, it is already possible to reach some of the target specifications. This method can be generalized in order to make automated calculations and thus to save time during the design phase. Furthermore, it is possible to improve the results by means of optimization algorithms using the g_m/I_d of the transistors as free choice parameters.

References:
[1] Jespers, P. (2009). *The gm/ID Methodology, a sizing tool for low-voltage analog CMOS Circuits: The semi-empirical and compact model approaches*(Vol. 29). Springer.
[2] Razavi, B. (2001). *Design of Analog CMOS Integrated Circuits*, McGraw-Hill,